

# Thor-P Gen2 Schematic Page Number

001_TITLE PAGE	047_THINK ENGINE 2(1/2)	093_BLANK
002_BLOCK DIAGRAM	048_THINK ENGINE 2(2/2)	094_BLANK
003_SYSTEM DEFINED	049_USB Type-A Port-A (AOU)	095_BLANK
004_Power State	050_USB Type-A Port-B	096_BLANK
005_Power tree	051_G-Sensor/TPM2.0	097_BLANK
006_CPU TGL-H: DDR4 CH-A	052_KB/Click PAD/Track Point/FP	098_BLANK
007_CPU TGL-H: DDR4 CH-B	053_FAN/IOB CONN/AC-IN LED	099_BLANK
008_CPU TGL-H: DDI/MISC/CLK/JTAG	054_SMB SW/Smart Card/EC Debug	100_Type C Adapter
009_CPU TGL-H: PCIE/DMI/TCP/DPIN	055_CardReader/SD Card for TpPv	101_DC-IN
010_CPU TGL-H: RSVD	056_BLANK froMXM CONN	102_BATTERY INPUT
011_CPU TGL-H: POWER	057_QN20P: PCI EXPRES/XTAL	103_BATTERY CHARGER
012_CPU TGL-H: GND	058_QN20P: FB CH.A/B	104_BLANK
013_PCH TGL-H: PCH Straps	059_QN20P: VRAM FBA	105_DC/DC VCC5M/VCC3M
014_PCH TGL-H: CLK/CNVI/DMI	060_QN20P: VRAM FBA_CAP	106_DC/DC VCC1R2A/VCC0R6B
015_PCH TGL-H: PCIE/USB/SPI/MISC	061_QN20P: VRAM FBB	107_DC/DC VCC2R5A
016_PCH TGL-H: GPIO (1/2)	062_QN20P: VRAM FBB_CAP	108_BLANK
017_PCH TGL-H: GPIO (2/2)	063_QN20P: OVRM GEN1/GEN2	109_DC/DC IMVP9
018_PCH TGL-H: POWER	064_QN20P: GPIO and I2C	110_DC/DC VCCPUCORE
019_PCH TGL-H: GND	065_QN20P: POWER	111_BLANK
020_RTC BATTERY/SPI FLASH/APS	066_QN20P: GND	112_BLANK
021_DDR4 CH-A PRIMARY	067_QN20P: DECOUPLING	113_BLANK
022_BLANK	068_QN20P: IFP A/B/C/D/E	114_VCCPUCORE_DECOUPLING
023_DDR4 CH-B PRIMARY	069_QN20P: STRAP and ROM	115_VCCPUCORE_AUX
024_BLANK	070_BLANK	116_VCCPCHCORE
025_THUNDERBOLT RETIMER A	071_SCREW HOLE	117_BLANK
026_BLANK	072_LOAD BOM	118_BLANK
027_BLANK	073_BLANK	119_DC/DC VCC1R8_SUS
028_Type-C PD Controller-1 (TBT)	074_BLANK	120_DC/DC VCCGFXCORE_D IC
029_BLANK	075_BLANK	121_DC/DC VCCGFXCORE_D
030_TBT Type-C CONN	076_BLANK	122_DC/DC VCC1R2VIDEO
031_BLANK	077_BLANK	123_CDC_VCC12
032_BLANK	078_BLANK	124_LOAD SW 1P8A
033_LCD/Camera/Touch CONN	079_BLANK	125_DC/DC VCC1R0VIDEO
034_HDMI2.0 Ret i nter and Conn	080_BLANK	126_LOAD SW VIDEO/3SUS
035_BLANK for HDMI LSPCON	081_BLANK	127_DISCHARGE CIRCUIT VIDEO
036_M.2 NVMe SSD Slot_1&2	082_BLANK	128_LOAD SW VCCST/VCCSTG
037_Blank for GEN4 SSD	083_BLANK	129_LOAD SW VCC3_SUS/TP
038_M.2 WLAN_1216	084_BLANK	130_BLANK LOAD SW LAN
039_M.2 WWAN/P-Sensor	085_BLANK	131_LOAD SW B
040_Intel LAN (I219)	086_BLANK	132_LOAD SW WWAN&WLAN
041_RJ45 CONN	087_BLANK	133_LOAD SW TOUCH/SSD
042_AUDIO SIP (ALC3287)	088_BLANK	134_LOAD SW VCC3_PD
043_HP/MIC/SPKR/Debug Port	089_BLANK	135_LOAD BOM
044_NPCX997KA0BX(1/3)	090_BLANK	
045_NPCX997KA0BX(2/3)	091_BLANK	
046_NPCX997KA0BX(3/3)	092_BLANK	

Thor-P GEN2 Block Diagram

Project Code: HT5B0 / HP5B0

Thor-P GEN2		
PLM Project Code	PCB	GPU
HP5B0 (P15V)	NMD551	QN20-M3
	NMD552	QN20-P1
		QN20-P3
HT5B0 (T15P)	NMD551	N18P

PCB Layer Stackup		
12L NM-C641 Rev : 0.3		
L1:	TOP	
L2:	GND1	
L3:	Signal1	
L4:	GND2	
L5:	Signal2	
L6:	GND3	
L7:	VCC1	
L8:	Signal3	
L9:	VCC2	
L10:	Signal4	
L11:	GND4	
L12:	BOTTOM	

INPUTS	OUTPUTS
Battery Charger	
RAT-PWR12	M-BAT-PWR
System DC/DC	
VINT20	VCC5M VCC3M
CPU DC/DC	
VINT20	VCCCPUCORE VCCGFXCORE_1 VCCSA
VCCCPU10	
VINT20	VCCCPU10
VCCIR05_SUS	
VCC5M	VCCIR0_SUS
VCCIR2A/VCC0R6B	
VINT20	VCC0R6B VCCIR2A
VCCIR8_SUS	
VCC5M	VCCIR8_SUS
VCC2R5A	
VCC5M	VCC2R5A
GFXCORE_D	
VINT20	VCCGFXCORE_D
VCCIR2VIDEO	
VCC5M	VCCIR2VIDEO
VCCIR0VIDEO	
VCC5M	VCCIR0VIDEO

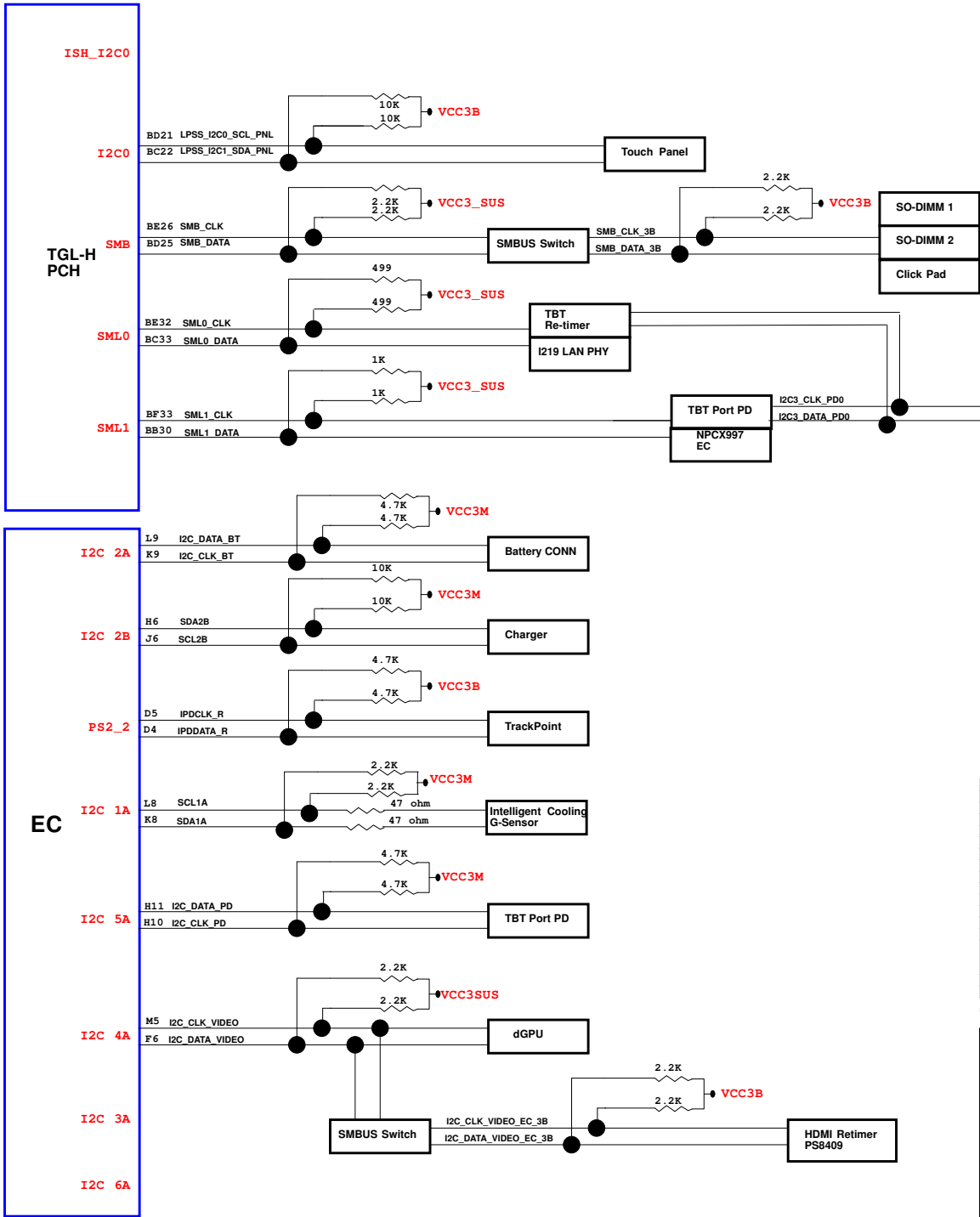
TP1  
Track Point

JKB1 Keyboard Conn.	RS1 / KSO
JCP1 Click Pad Conn.	PS2 SMB PCH
LED LED1: Charger (White & Orange) LED2: AC-In (White) LED3: Cable Logo (Red)	PWR
PU001 Charger	I2C
P0001 BATT Conn.	I2C
U2801 PD Controller	I2C
U5101 G Sensor	I2C
U3401 HDMI2.0 Re-timer	I2C
UP01 dGPU NVIDIA QN20-P1 / QN20-P3	I2C
U2801 PD Controller	I2C SMB 1 PCH
JCFAN1 Fan Conn.	FWM
Thermal Sensor RT4501: BOT: CPU DCDC RT4504: BOT: Ambient RT4505: BOT: GPU DCDC RT4507: BOT: DRP DCDC RT4603: BOT: SSD	GPIO
U2801 Think Engine	SPI

U1CD1 LCD 15.6" FHD/UHD LCD Touch	eDP x4 I2C PCH
U3401 HDMI2.0 Re-timer	DDIB x4
UP01 dGPU NVIDIA P1 / P3 / N18P / M3	PCIe 8-15
U4101 RJ45 LAN Conn.	MDI
U4002 LAN	PCIE 5 SMB 0 PCH
U5501 Card Reader	PCIE 8
SSD Conn. JSSD1 M.2 SSD Conn. JSSD2 M.2 SSD Conn.	PCIE 9-12 PCIE 17-20
U5102 TPM	SPI
U2002 SPI SW	Quad SPI Quad SPI
U4402 EC ROM	Quad SPI Quad SPI
U2001 BIOS ROM	Quad SPI Quad SPI
U4401 EC	Quad SPI Quad SPI
U4401 EC	Quad SPI Quad SPI

U1 CPU Intel Tiger Lake H 135W	DMI x8
U2 PCH Intel Tiger Lake H 135W	DMI x8

U1801 WLAN	CNVF
U4201 Audio Codec	HDA
JUSB1 USB Type-A Conn. A	USB 2.7 USB 2.2
JUSB2 USB Type-A Conn. B	USB 2.1 USB 2.1
JWWAN1 WWAN Conn.	USB 2.2 PCIe 7
JFP1 Finger Print Conn.	USB 2.3
JCAM1 Camera Conn.	USB 2.4
JSC1 Smart Card Conn.	USB 2.9
U3004 Debug Part SW	USB 2.5
U2501 Thunderbolt Re-timer ROM	EC
U2502 Thunderbolt Re-timer	TCP0 x2 SMB 1 CPU
JHDM11 USB Type-C Conn.	USB 2.0 USB 3.0 CC
U2801 PD Controller	GPIO4: Force PWR PD GPIO1: HPD GPIO8: OC GPIO2: ProHot GPIO3: CPU
U2802 PD Controller ROM Combine with EC	GPIO2: ProHot GPIO3: CPU
JUSB1 RTC Conn.	SMB 8



PCH I2C0 address

Device	Address (7bits)	Address (8bits)
Touch Panel	I/O+ELAN 0x10 BOE+G2Touch 0x10	I/O+ELAN 0x20 (W) / 0x21 (R) BOE+G2Touch 0x20 (W) / 0x21 (R)

PCH SMB address

Device	Address (7bits)	Address (8bits)
CH-A DDR DIMM1	0x50	0xA0 (W) / 0xA1 (R)
CH-B DDR DIMM2	0x51	0xA2 (W) / 0xA3 (R)
Click Pad	0x2C	0x58 (W) / 0x59 (R)

PCH SML0 address

Device	Address (7bits)	Address (8bits)
Intel Lan I219	0x64	0xC8 (W) / 0xC9 (R)
TBT Re-timer	0x20	0x40 (W) / 0x41 (R)

PCH SML1 address

Device	Address (7bits)	Address (8bits)
PD Controller (Part A)	0x23	0x46 (W) / 0x47 (R)

PD Controller

Device	Address (7bits)	Address (8bits)
TBT Re-timer	0x52	0xA4 (W) / 0xA5 (R)

EC SMB1A address

Device	Address (7bits)	Address (8bits)
G-Senor (KX022-1020)	0x1E	0x3C (W) / 0x3D (R)
G-Senor (LIS2DWLTR)	0x18	0x30 (W) / 0x31 (R)

EC SMB2A address

Device	Address (7bits)	Address (8bits)
Battery	0x16	0x2C (W) / 0x2D (R)

EC SMB2B address

Device	Address (7bits)	Address (8bits)
Charge Controller	0x12	0x24 (W) / 0x25 (R)

EC SMBus4 address

Device	Address (7bits)	Address (8bits)
HDMI Re-timer	0x10 - 0x2F	0x20 (W) / 0x21 (R) - 0x5E (W) / 0x5F (R)
DGPU	0x4F	0x9E

EC SMBus5 address

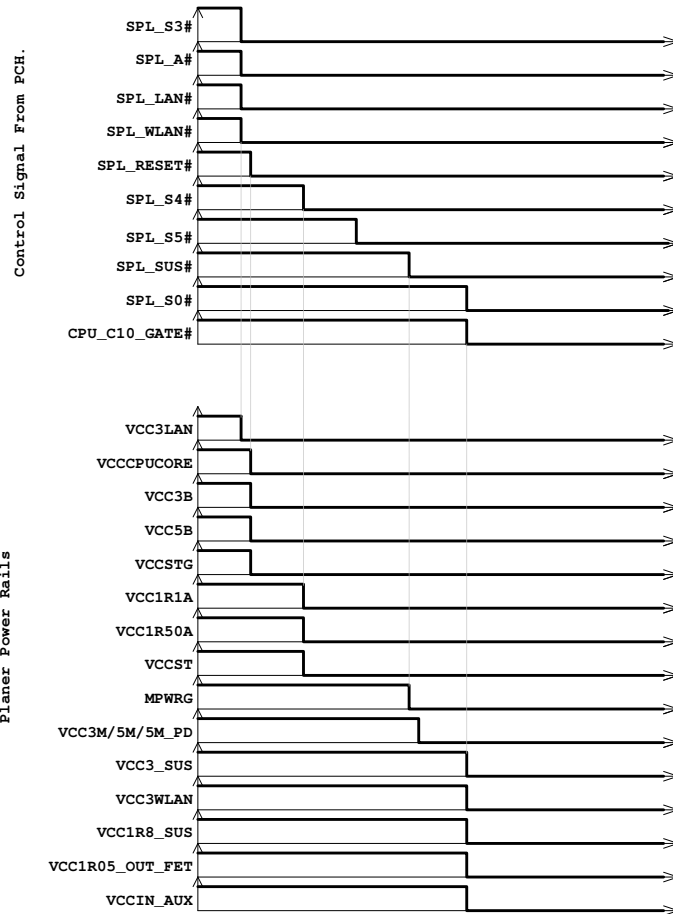
Device	Address (7bits)	Address (8bits)
PD Controller (Part A)	0x20	0x40 (W) / 0x41 (R)

Port	Device	Power	CLK	DATA	Address (7bits)	Address (8bits)
PCH I2C0	Touch Panel (I/O+ELAN)	VCC3B	LPSS_I2C1_SCL_PNL	LPSS_I2C1_SDA_PNL	0x10	0x20 (W) / 0x21 (R)
	Touch Panel (BOE+G2 Touch)				0x50	0xA0 (W) / 0xA1 (R)
PCH SMB	SO-DIMM1	VCC3_SUS	SMB_CLK	SMB_DATA	0x51	0xA2 (W) / 0xA3 (R)
	SO-DIMM2				0x2C	0x58 (W) / 0x59 (R)
PCH SML0	Intel Lan I219	VCC3_SUS	SML0_CLK	SML0_DATA	0x64	0xC8 (W) / 0xC9 (R)
	TBT Re-timer				0x20	0x40 (W) / 0x41 (R)
PCH SML1	PD Controller (Part A)	VCC3_SUS	SML1_CLK	SML1_DATA	0x23	0x46 (W) / 0x47 (R)
	TBT Re-timer	VCC3_LDO_PD1	I2C3_CLK_PD0	I2C3_DATA_PD0	0x52	0xA4 (W) / 0xA5 (R)
EC SMB1A	G-Senor (KX022-1020)	VCC3M	I2C_CLK_GSENSE	I2C_DATA_GSENSE	0x1E	0x3C (W) / 0x3D (R)
	G-Senor (LIS2DWLTR)				0x18	0x30 (W) / 0x31 (R)
EC SMB2A	Battery	VCC3M	I2C_CLK_BT	I2C_DATA_BT	0x16	0x2C (W) / 0x2D (R)
EC SMB2B	Charger	VCC3M	I2C_CLK_CHARGE	I2C_DATA_CHARGE	0x12	0x24 (W) / 0x25 (R)
					0x20	0x40 (W) / 0x41 (R)
EC SMB4A	HDMI Retimer	VCC3B	I2C_CLK_VIDEO_EC_3B	I2C_DATA_VIDEO_EC_3B	0x10 - 0x2F	0x5E (W) / 0x5F (R)
	DGPU	VCC1R8VIDEO	GPU_I2CS_SCL	GPU_I2CS_SDA	0x4F	0x9E (W) / 0x9F (R)
EC SMB5A	PD Controller (Part A)	VCC3_PD	I2C_CLK_PD	I2C_DATA_PD	0x20	0x40 (W) / 0x41 (R)

TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	MT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	Suspend-to-RAM (STR)
G1	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	Suspend-to-Disk (STD)
	Deep S4	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	
	Deep S5	M-OFF	ON	ON	OFF	OFF	OFF	OFF		Soft Off
	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

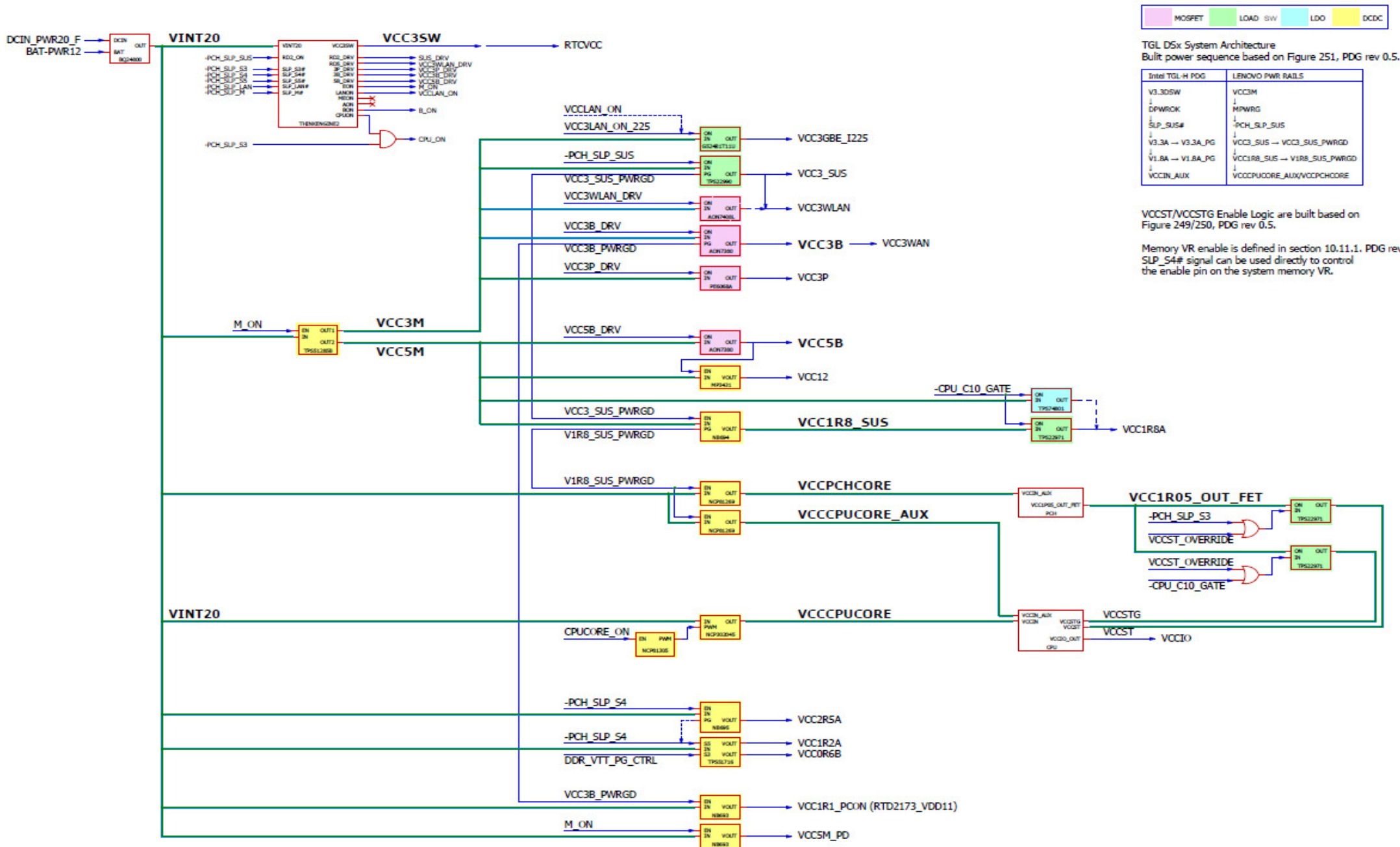
Timing Diagram for S0/M0 to G3 [Deep Sx]  
Based on planer power rail.



Power Rail Name	Voltage Range	Enable/Control Signal	Sx Power State			
			S0	S3	S4	S5
VINT20	9-20V	NA	ON	ON	ON	ON
RTCVCC	3-3.3V	NA	ON	ON	ON	ON
VCC3SW	3.3V	NA	ON	ON	ON	ON
VCC3M	3.3V	M_ON	ON	ON	ON	ON
VCC3LAN	3.3V	VCC3LAN_DRV	ON	OFF	OFF	OFF
VCC3_SUS	3.3V	SUS_DRV	ON	ON	ON	ON
VCC3WLAN	3.3V	NA	ON	ON	ON	ON
VCC3B	3.3V	VCC3B_DRV	ON	OFF	OFF	OFF
VCC3P	3.3V	VCC3P_DRV	ON	OFF	OFF	OFF
VCC5M	5V	M_ON	ON	ON	ON	ON
VCC5B	5V	VCC5B_DRV	ON	OFF	OFF	OFF
VCC1R8_SUS	1.8V	VCC3_SUS-PWRGD	ON	ON	ON	ON
VCC1R8A	1.8V	-CPU_C10_GATE	ON	ON	ON	ON
VCCPCHCORE	2 bit VID	V1R8_SUS_PWRGD	ON	ON	ON	ON
VCCST	1.05V	VCCST_OVERRIDE OR -PCH_SLP_S3	ON	OFF	OFF	OFF
VCCSTG	1.05V	VCCST_OVERRIDE OR -CPU_C10_GATE	ON	OFF	OFF	OFF
VCCCPUCORE	SVID	CPUCORE_ON	ON	OFF	OFF	OFF
VCC1R1A	1.1V	-PCH_SLP_S4	ON	ON	OFF	OFF
VCC5R0A	5V	-PCH_SLP_S4*	ON	ON	OFF	OFF
VCC5M_PD	5V	M_ON	ON	ON	ON	ON
VCC1R1_PCON	1.1V	TBD				

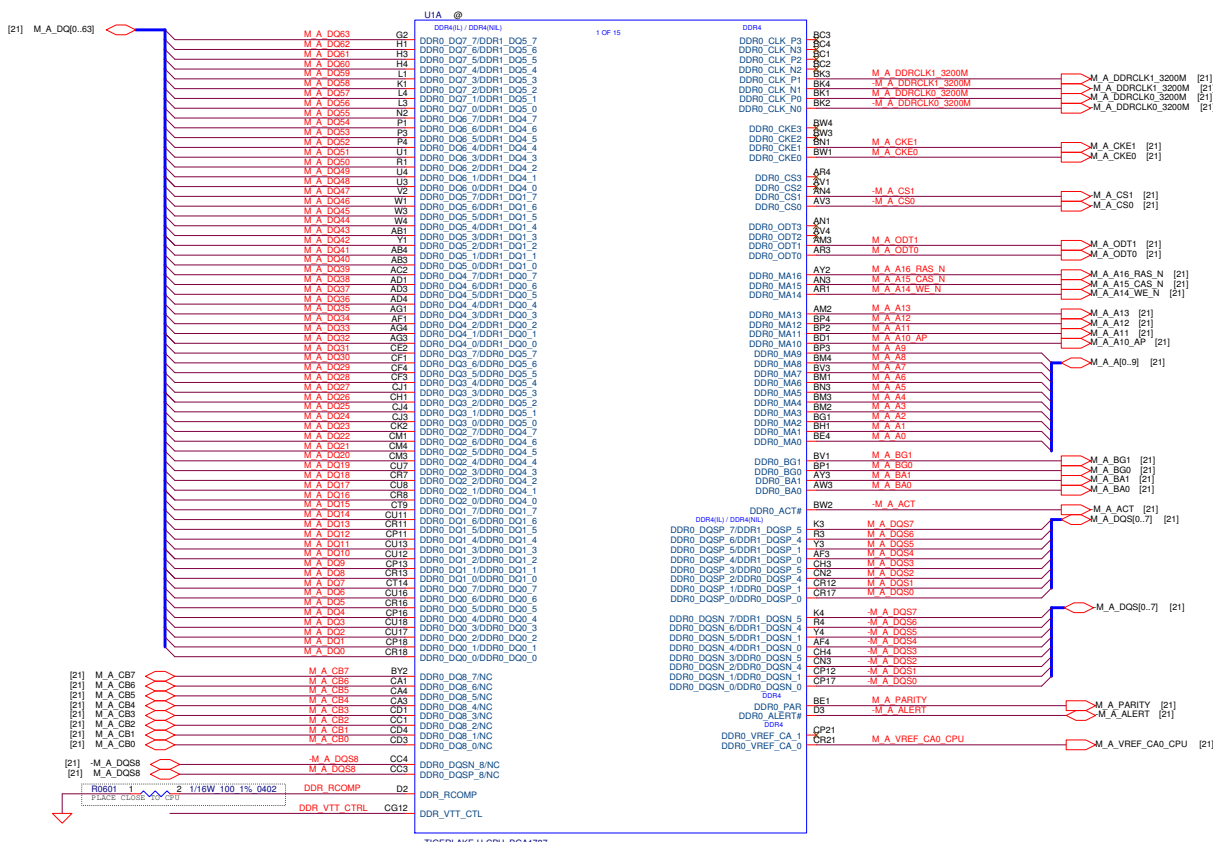
Not fixed yet.  
Please refer to latest TGL-H PDG.

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Power Tree

CPU DDR4 CH-A

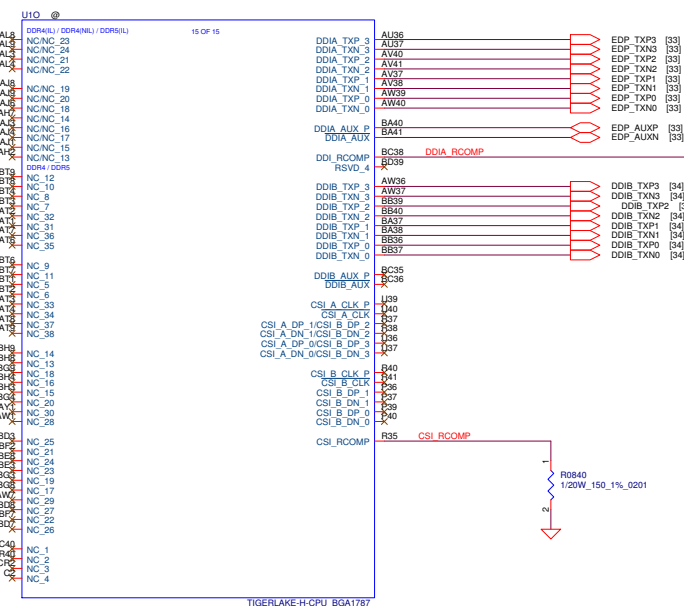


CPU DDR4 CH-B



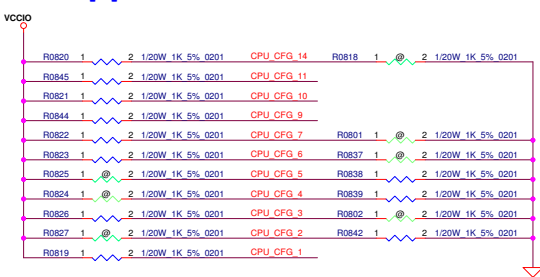


## CPU DDI/MISC/CLK/JTAG

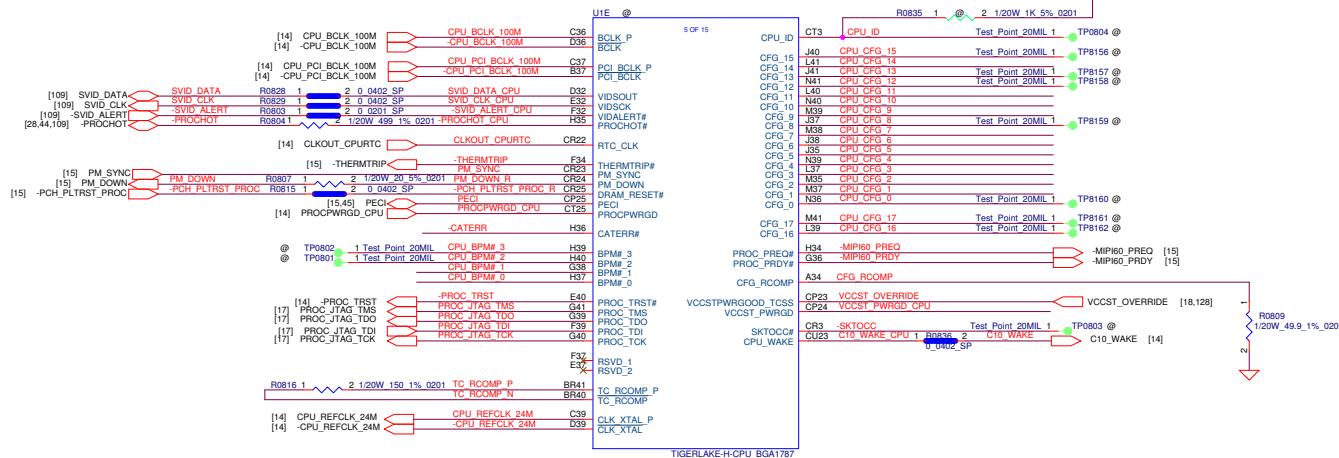
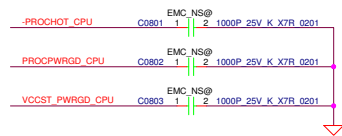


eDP panel

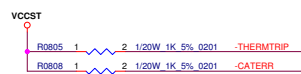
HDMI



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## CPU Sideband PU



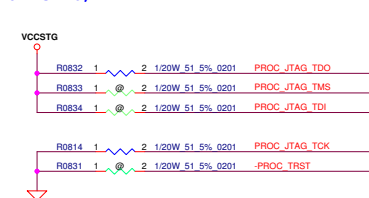
## SVID PU



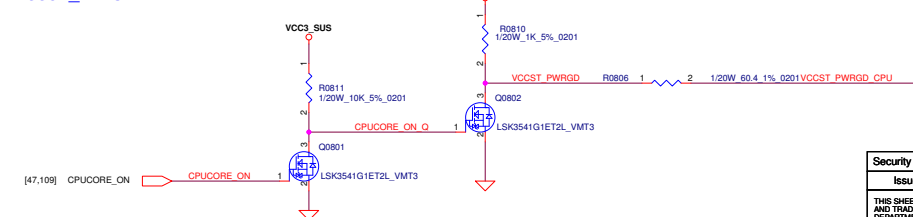
BPM#	PU
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## JTAG PU/PD



## VCCST PWRGD




## PRDY PU



### CFG pin assignment

0	RSVD
1	RSVD(Pull-up)
2	PEG x16 Lane Reversal 1:Normal 0:Reversed <span style="float: right;">&lt;----- Logic</span>
3	RSVD(Pull-up)
4	eDP enable 0:Enabled 1:Disabled <span style="float: right;">&lt;----- Logic</span>
6:5	PCI Express Bifurcation 00: 1x8, 2x4 PCI Express 01: Reserved 10: 2x8 PCI Express 11:1x16 PCI Express <span style="float: right;">&lt;----- QN20-P1</span>
7	RSVD --> PDG Rev1.0 update
8	RSVD
11:9	RSVD(Pull-up)
13:12	RSVD
14	PEG60(PCIE4) Lane Reversal 1:Normal 0:Reversed <span style="float: right;">&lt;----- Logic no use</span>
17:15	RSVD

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	CPU TGL-H : DD/MISC/CLK/JTAG	
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Custom	Monday, May 19, 2020		Sheet 8 of 136		

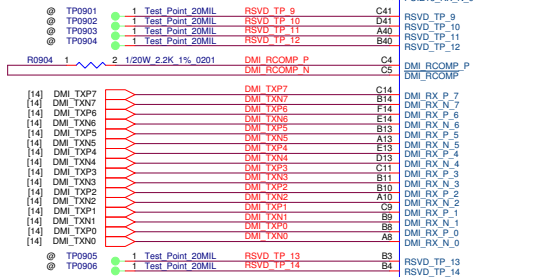


# CPU PCIE/DMI/TCP/DPIN

[57] PEG\_RXP[7:0]  
[57] PEG\_RXN[7:0]

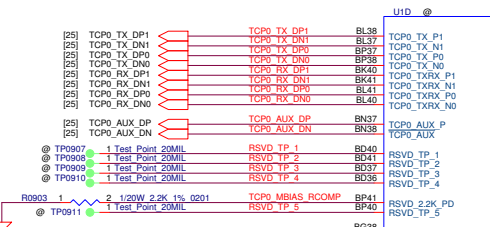
GPU

PEG\_TXP[7:0] [57]  
PEG\_TXN[7:0] [57]



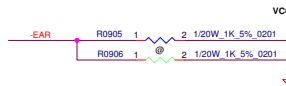
TIGERLAKE-H-CPU\_BGA1787

TBT Port A  
(JTBT1)



TIGERLAKE-H-CPU\_BGA1787

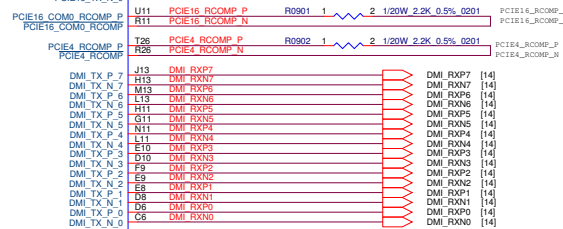
-EAR



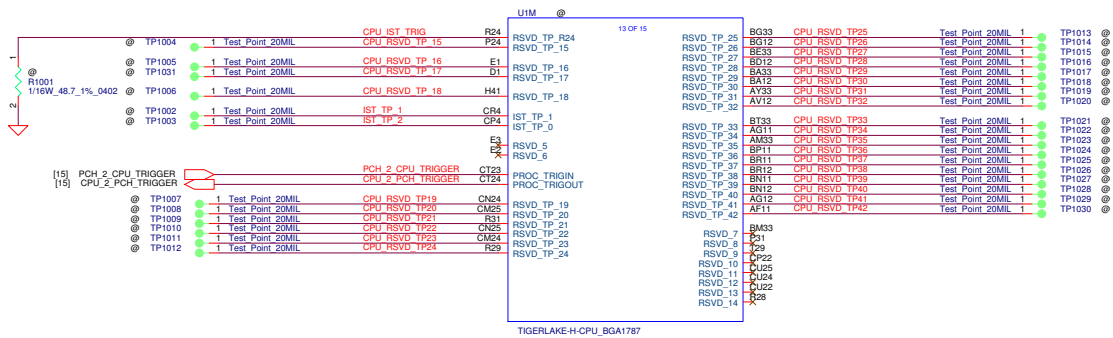
-EAR pin assignment  
Stall reset sequence after PCU PLL lock until de-asserted  
1: Normal (No stall)  
0: Stall

[17] PROC\_AUDIO\_SDI\_CPU R9913 1 2 1/20W 20.5% Q201 PROC\_AUDIO\_SDI\_CPU R A32  
[17] PROC\_AUDIO\_SDO\_CPU A31 AUDOUT  
[17] PROC\_AUDIO\_CLK\_CPU C953 1 2 10P 25V J\_NPO Q201 PROC\_AUDIO\_CLK\_CPU D R9914 1 2 1/20W 0.5% Q201 AUDCLK

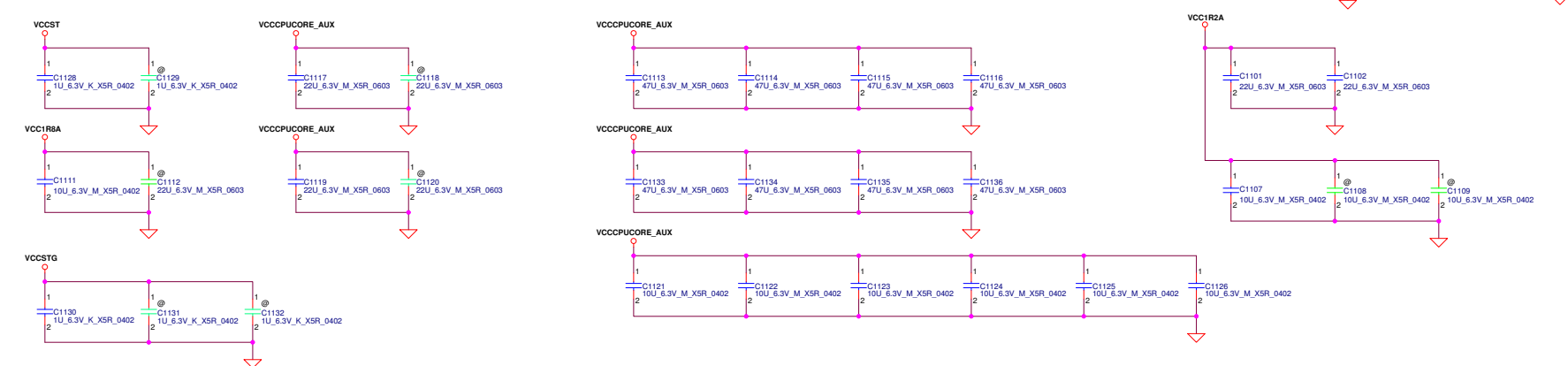
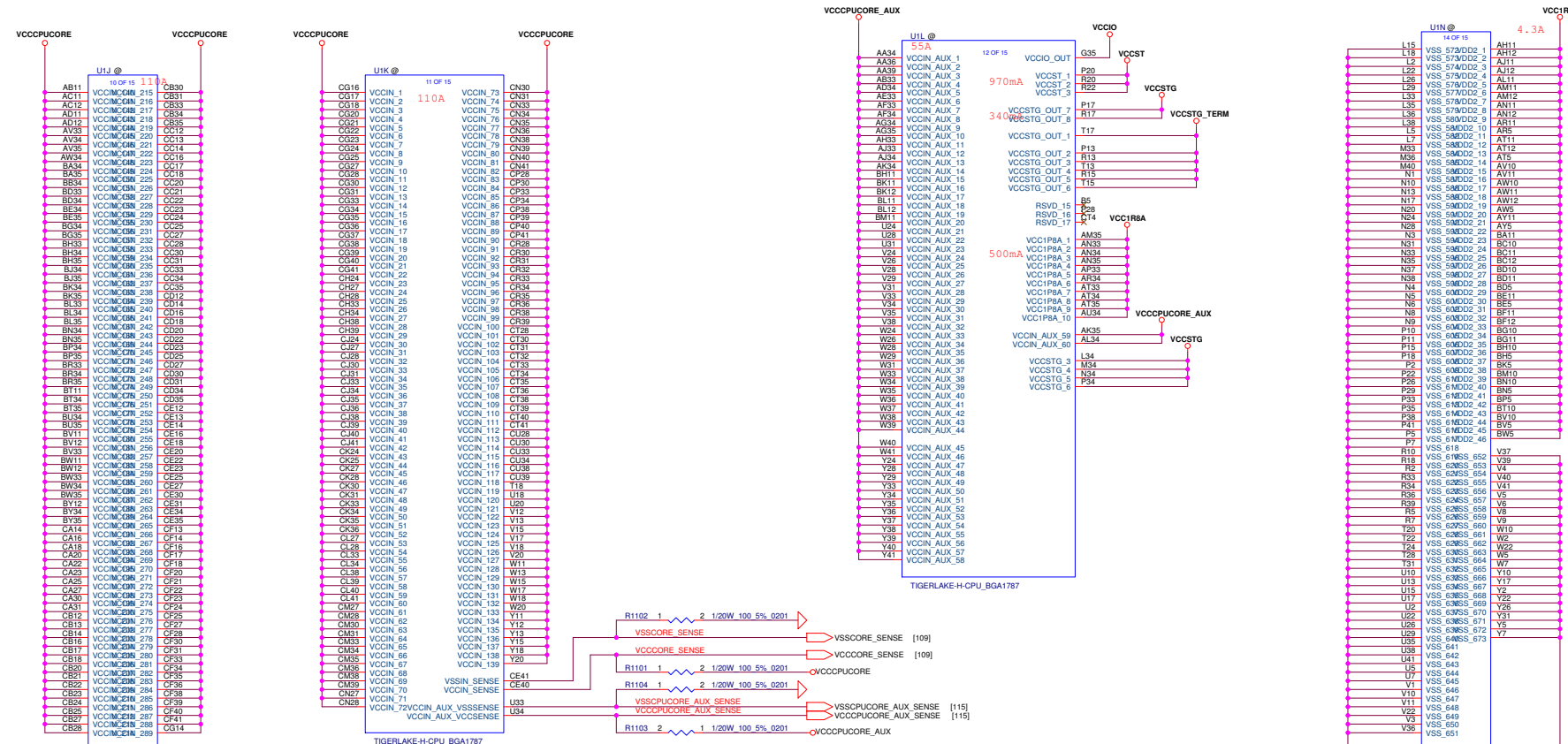
TIGERLAKE-H-CPU\_BGA1787



CPU RSVD



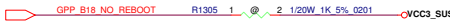
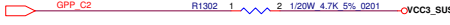
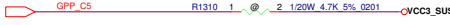
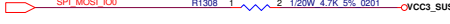



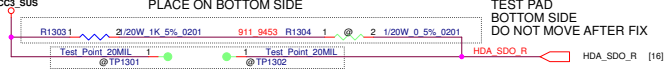


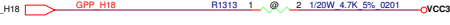
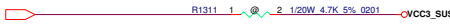


CPU POWER



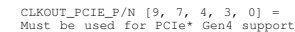
[illegible][illegible]

# PCH Straps

Reference 615985-tgl-rkl-pch-eds-vol1-rev0p7, Table17

Signal	Usage	Comment	Setting
GPP_B14/SPKR	Top Swap Override	0 = Disable "TOP Swap" Mode (Default) 1 = Enable "TOP Swap" Mode This strap has a 20k internal PD	This strap is set by EC. See "BIOS_HEALING" signal
GPP_B18/GSPI0_MOSI	No Reboot	0 = Disable "No Reboot" Mode (Default) ← Logic 1 = Enable "No Reboot" Mode This strap has a 20k internal PD	[17] GPP_B18_NO_REBOOT 
GPP_C2/SMBALERT#	TLS Confidentiality	0 = Disable ME Crypto TLS(Default) 1 = Enable ME Crypto TLS with Confidentiality ← Logic This strap has a 20k internal PD	[17] GPP_C2 
GPP_C5/SML0ALERT#	eSPI Disable	0 = Enable eSPI (Default) ← Logic 1 = Disable eSPI This strap has a 20k internal PD	[17] GPP_C5 
SPI0_MOSI	Reserved	External pull-up is required Recommend 4.7K PU	[15,20,51] SPI_MOSI_I00 
GPP_G9/ISH_SPI_CLK/ DDP3_CTRLDATA/ GSPi2_CLK/ TBT_LSX2_RXD	DDP3 I2C/TBT_LSX2/ BBSB_LS2 pins VCC configuration	0 = DDP3 I2C/TBT_LSX2/BBSB_LS2 pins at 1.8V ← Logic 1 = DDP3 I2C/TBT_LSX2/BBSB_LS2_TX pins at 3.3V This strap has a 20k internal PD	NC
GPP_G11/ ISH_SPI_MOSI/ DDP4_CTRLDATA/ GSPi2_MOSI/ TBT_LSX3_RXD	DDP4 I2/TBT_LSX3/ BSSB_LS3 pins VCC configuration	0 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 1.8V ← Logic 1 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 3.3V This strap has a 20k internal PD	NC
GPP_B23/ SML1ALERT#/ PCHHOT#	CPUNSSC Clock Frequency	0 = 38.4 MHz clock (direct from crystal) (Default) ← Logic 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) This strap has a 20k internal PD	[17] GPP_B23 
SPI0_IO2	Reserved	External pull-up is required ← Logic Recommend 100K if pulled up to 3.3V	[15,20] SPI_IO2 
SPI0_IO3	Reserved	External pull-up is required ← Logic Recommend 100K if pulled up to 3.3V	[15,20] SPI_IO3 
GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	0 = Enable security measures defined in the Flash Descriptor (Default) 1 = Disable Flash Descriptor Security (override) This strap has a 20k internal PD	 PLACE ON BOTTOM SIDE TEST PAD BOTTOM SIDE DO NOT MOVE AFTER FIX
GPP_H12/ SML2ALERT#	eSPI Flash Sharing Mode	0 = Master Attached Flash Sharing (MAFS) enabled ← Logic (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled This strap has a 20k internal PD	[16] GPP_H12 
GPP_H15 / SML3ALERT#	JTAG ODT Disable	0 = JTAG ODT is disabled (Default) 1 = JTAG ODT is enabled ← Logic This strap has a 20k internal PD	[16] GPP_H15 
GPP_H18 / SML4ALERT#	VCCSPI Voltage Configuration	0 = VCCSPI at 3.3 V (Default) ← Logic 1 = VCCSPI at 1.8 V This strap has a 20k internal PD	[16] GPP_H18 
GPP_G13 / DDP1_CTRLDATA / TBT_LSX0_RXD	DDP1 I2C/TBT_LSX0 /BSSB_LS0 pins VCC configuration	0 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V ← Logic 1 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V This strap has a 20k internal PD	[17,25] TBT_LSX0_RXD 
GPP_G15 / DDP2_CTRLDATA / TBT_LSX1_RXD	DDP2 I2C / TBT_LSX1 /BSSB_LS01pins VCC configuration	0 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V ← Logic 1 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V This strap has a 20k internal PD	NC
DBG_PMODE	Reserved	This strap should sample high This strap has a 20k internal PU	NC
GPP_J2/ CNV_BRI_DT / UART0_RTS#	XTAL_Frequency Selection	0 = 38.4 MHz (Default) ← Logic 1 = 24 MHz This strap has a 20k internal PD	[16] BRI_DT_CNVI_R  PD exists in WLAN page (not for strap function)
GPP_J4 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	0 = Integrated CNVi enabled ← CNVi 1 = Integrated CNVi disabled ← Discrete This strap doesn't have an internal PU or PD. A weak external pull-up is required.	PU exists in WLAN page It should be near the WLAN M.2 CNVi module has PD and strap value changes depends on type of module
GPP_B22 / GSPi1_MOSI	Boot BIOS Strap (BBS)	0 = BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF) ← Logic 1 = BIOS fetches are routed to the eSPI Peripheral Channel This strap has a 20k internal PD	[17] GPP_B22 
GPD7	Reserved	This strap should sample LOW This strap has a 20k internal PD	NC(Used only as GPIO)

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[illegible]

SUSCLK  
0 ohm placeholder is recommended, but not mandatory.  
If failing device Over/Undershoot, a 33 ohm resistor can be  
stuffed.



VCC1R2A

R1409 1 2 1/20W 470 1% 0201 -DRAMRST

R1402 1 2 1:20W 1M 5% 0201 MPWRG

R1410 1 2 1:20W 100K 1% 0201 -PCH SLP WLAN

R1411 1 2 1:20W 100K 1% 0201 -PCH SLP M


R1412 1 2 1:20W 100K 1% 0201 -PCH SLP S3

R1413 1 2 1:20W 100K 1% 0201 -PCH SLP S4

R1414 1 2 1:20W 100K 1% 0201 -PCH SLP S5

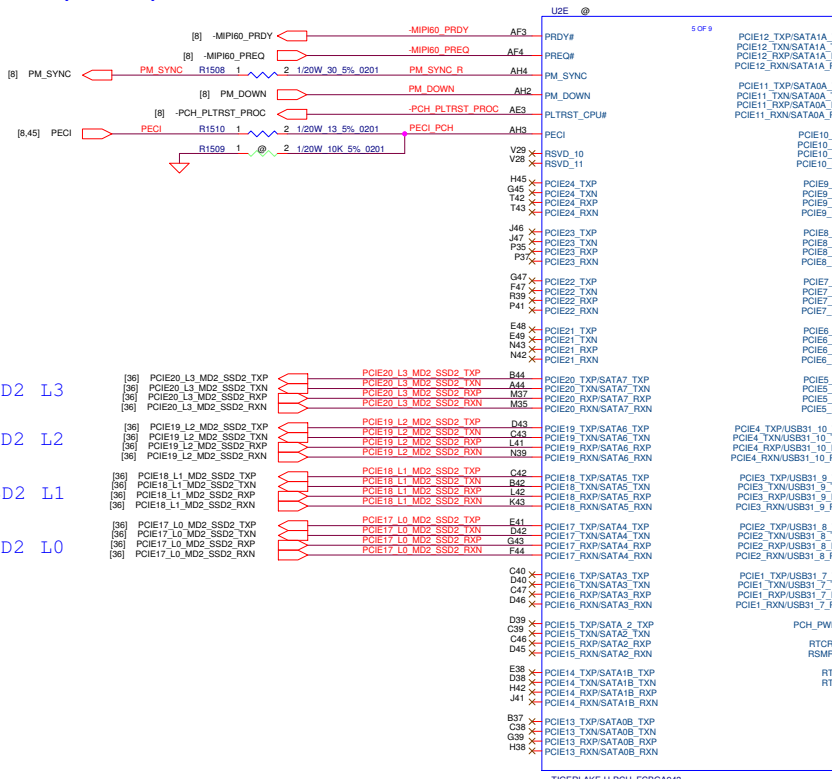
[25] -RT PERST -PLTRST\_PCH [17,33,36,39,40,47,51,55,64]

TGL platform: Connect to PCH PLT\_RST# as default and reserve the connection to PCH GPIO GPD\_7.

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# PCH PCIE/USB2&3/SPI/MISC



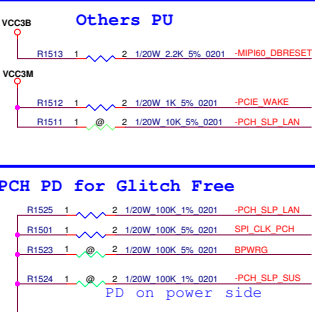
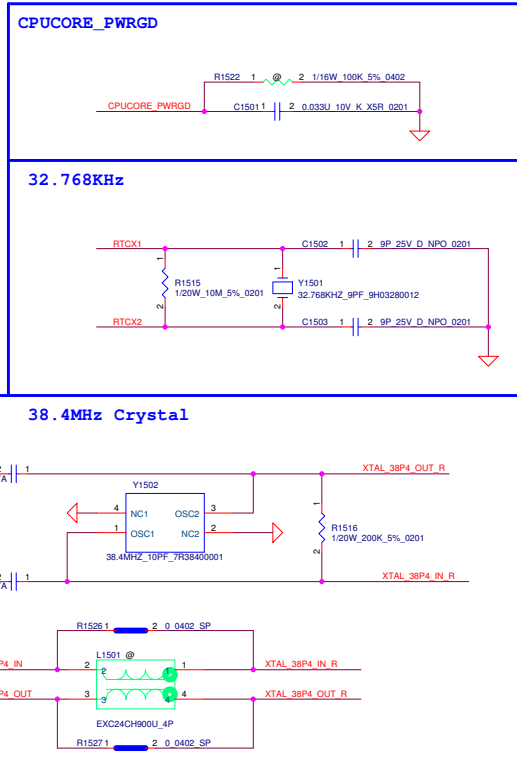
M.2 SSD2 L3  
M.2 SSD2 L2  
M.2 SSD2 L1  
M.2 SSD2 L0

Planar Type-C  
WWAN  
USB Type-A  
USB Type-A (AOU)  
Planar Type-C  
Smart Card  
Touch panel  
USB Type-A portB  
TBT PortB  
TBT PortA  
Camera  
Finger print  
WWAN  
USB Type-A (AOU)

PCIe Port Assignment	
Port Number	Function
Port 5	GbE
Port 6	
Port 7	WWAN
Port 8	SD Card
Port 9-12	M.2 SSD1
Port 17-20	M.2 SSD2

USB3 Port Assignment	
Port Number	Function
Port 1	USB Type-A (AOU)
Port 2	USB Type-A Port B

USB2 Port Assignment	
Port Number	Function
Port 1	USB Type-A (AOU)
Port 2	WWAN
Port 3	Fingerprint
Port 4	Camera
Port 5	TBT Port A
Port 6	
Port 7	USB Type-A Port B
Port 8	
Port 9	Smart Card
Port 10	
Port 12	





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# PCH GPIO(1/2)

**Others PU**

- VCC1R8\_SUS
- VCC3\_SUS

**-USB OC PU & EMC CAP**

- USB\_USBA\_OC2
- USB\_TCSS\_OC0
- USB\_USBB\_OC1
- USB\_USBA\_OC3

**CORE\_VID**

- CPUCORE\_AUX\_VID1
- PCHCORE\_VID1
- CPUCORE\_AUX\_VID0
- PCHCORE\_VID0

**HDA Signals**

- HDA\_SYNC\_R
- HDA\_RST\_R
- HDA\_BCLK

**For CNVi**

- BRI\_RSP\_CNVI
- RGI\_RSP\_CNVI

**PWRSW**

- PWRSW\_EC

**GPU Control Pin**

- GPU\_RST

**PLANARID**

PLANAR ID	3	2	1	0
R1623	R1624	R1625	R1626	
1	NA	NA	NA	
0	ASM	ASM	ASM	ASM

LEVEL	PLANARID[3..0]	CPU	PCH
PDV	-----	-----	-----
EVT	0001b	TBD	TBD
FVT	0010b	TBD	TBD
SIT	0011b	TBD	TBD
SVT			

**Security Classification**

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**Title**

PCH TGL-H : GPIO (1/2)

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**Size**

Document Number

**Date**

Monday, May 10, 2021

**Sheet**

16 of 136

**Rev**

0.3

# PCH GPIO(1/2)

**Others PU**

- VCC1R8\_SUS: R1652 1 2 1/20W 10K 5% 0201 -LID\_CLOSE\_R
- VCC3\_SUS: R1634 1 2 1/20W 10K 5% 0201 -PMC\_ALERT

**-USB OC PU & EMC CAP**

- USB\_USBA\_OC2: R1657 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC0: R1608 1 2 1/20W 10K 5% 0201
- USB\_USBB\_OC1: R1609 1 2 1/20W 10K 5% 0201
- USB\_USBA\_OC3: R1611 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC5: C16011 @ 2 1000P 25V K X7R 0201
- USB\_USBB\_OC5: C16031 @ 2 1000P 25V K X7R 0201
- USB\_USBA\_OC5: C16021 @ 2 1000P 25V K X7R 0201

**CORE\_VID**

- CPUCORE\_AUX\_VID1: R16351 2 0 0201 SP
- PCHCORE\_VID1: R16361 2 0 0201 SP
- CPUCORE\_AUX\_VID0: R16371 2 0 0201 SP
- PCHCORE\_VID0: R16381 2 0 0201 SP

**HDA Signals**

- HDA\_SYNC\_R: R1617 1 2 1/20W 1K 5% 0201
- HDA\_RST\_R: C1605 1 2 2P 25V C NPO 0201
- HDA\_BCLK: R1604 1 2 47P 25V J NPO 0201

**For CNVi**

- BRI\_RSP\_CNVI: R1602 1 2 1/16W 20K 1% 0402
- RGI\_RSP\_CNVI: R1603 1 2 1/16W 20K 1% 0402

**PWR5W**

- PWR5W\_EC: R1649 1 2 1/20W 10K 5% 0201
- PWR5W\_EC: D1602 2 1 RBS21CM-30T2R VMN2M-2

**GPU Control Pin**

- GPU\_RST: R1627 1 2 1/20W 10K 5% 0201
- GPU\_RST: R1630 1 2 1/20W 100K 5% 0201

**PLANARID**

- PLANARID3: R1623 1 2 1/20W 0 5% 0201
- PLANARID2: R1624 1 2 1/20W 0 5% 0201
- PLANARID1: R1625 1 2 1/20W 0 5% 0201
- PLANARID0: R1626 1 2 1/20W 0 5% 0201

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Issued Date: 2019/12/26

Deciphered Date: yyyy/mm/dd

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

Sheet: 16 of 136

Rev: 0.3

# PCH GPIO(1/2)

**Others PU**

- VCC1R8\_SUS: R1652 1 2 1/20W 10K 5% 0201 -LID\_CLOSE\_R
- VCC3\_SUS: R1634 1 2 1/20W 10K 5% 0201 -PMC\_ALERT

**-USB OC PU & EMC CAP**

- USB\_USBA\_OC2: R1657 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC0: R1608 1 2 1/20W 10K 5% 0201
- USB\_USBB\_OC1: R1609 1 2 1/20W 10K 5% 0201
- USB\_USBA\_OC3: R1611 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC5: C16011 @ 2 1000P 25V K X7R 0201
- USB\_USBB\_OC5: C16031 @ 2 1000P 25V K X7R 0201
- USB\_USBA\_OC5: C16021 @ 2 1000P 25V K X7R 0201

**CORE\_VID**

- CPUCORE\_AUX\_VID1: R16351 2 0 0201 SP
- PCHCORE\_VID1: R16361 2 0 0201 SP
- CPUCORE\_AUX\_VID0: R16371 2 0 0201 SP
- PCHCORE\_VID0: R16381 2 0 0201 SP

**HDA Signals**

- HDA\_SYNC\_R: R1617 1 2 1/20W 1K 5% 0201
- HDA\_RST\_R: C1605 2 2P 25V C NPO 0201
- HDA\_BCLK: R1604 1 2 47P 25V J NPO 0201

**For CNVi**

- BRI\_RSP\_CNVI: R1602 2 1/16W 20K 1% 0402
- RGI\_RSP\_CNVI: R1603 2 1/16W 20K 1% 0402

**PWR5W**

- PWR5W\_EC: R1649 1 2 1/20W 10K 5% 0201
- PWR5W\_EC: D1602 2 1 RBS21CM-30T2R VMN2M-2

**GPU Control Pin**

- GPU\_RST: R1627 1 2 1/20W 10K 5% 0201
- GPU\_RST: R1630 1 2 1/20W 100K 5% 0201

**PLANARID**

- PLANARID3: R1623 1 2 1/20W 0 5% 0201
- PLANARID2: R1624 1 2 1/20W 0 5% 0201
- PLANARID1: R1625 1 2 1/20W 0 5% 0201
- PLANARID0: R1626 1 2 1/20W 0 5% 0201

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LC Future Center Secret Data

Issued Date: 2019/12/26

Deciphered Date: yyyy/mm/dd

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

Sheet: 16 of 136

Rev: 0.3

# PCH GPIO(1/2)

**Others PU**

- VCC1R8\_SUS: R1652 1 2 1/20W 10K 5% 0201 -LID\_CLOSE\_R
- VCC3\_SUS: R1634 1 2 1/20W 10K 5% 0201 -PMC\_ALERT

**-USB OC PU & EMC CAP**

- USB\_USBA\_OC2: R1657 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC0: R1608 1 2 1/20W 10K 5% 0201
- USB\_USBB\_OC1: R1609 1 2 1/20W 10K 5% 0201
- USB\_USBA\_OC3: R1611 1 2 1/20W 10K 5% 0201
- USB\_TCSS\_OC5: C16011 @ 2 1000P 25V K X7R 0201
- USB\_USBB\_OC5: C16031 @ 2 1000P 25V K X7R 0201
- USB\_USBA\_OC5: C16021 @ 2 1000P 25V K X7R 0201

**CORE\_VID**

- CPUCORE\_AUX\_VID1: R1635.1 2 0.0201 SP
- PCHCORE\_VID1: R1636.1 2 0.0201 SP
- CPUCORE\_AUX\_VID0: R1637.1 2 0.0201 SP
- PCHCORE\_VID0: R1638.1 2 0.0201 SP

**HDA Signals**

- HDA\_SYNC\_R: R1617 1 2 1/20W 1K 5% 0201
- HDA\_RST\_R: C1605 1 2 2P 25V C NPO 0201
- HDA\_BCLK: R1604 1 2 47P 25V J NPO 0201

**For CNVi**

- BRI\_RSP\_CNVI: R1602 1 2 1/16W 20K 1% 0402
- RGI\_RSP\_CNVI: R1603 1 2 1/16W 20K 1% 0402

**PWR5W**

- PWR5W\_EC: R1649 1 2 1/20W 10K 5% 0201
- PWR5W\_EC: D1602 2 1 RBS21CM-30T2R VMN2M-2

**GPU Control Pin**

- GPU\_RST: R1627 1 2 1/20W 10K 5% 0201
- GPU\_RST: R1630 1 2 1/20W 100K 5% 0201

**PLANARID**

- PLANARID3: R1623 1 2 1/20W 0.5% 0201
- PLANARID2: R1624 1 2 1/20W 0.5% 0201
- PLANARID1: R1625 1 2 1/20W 0.5% 0201
- PLANARID0: R1626 1 2 1/20W 0.5% 0201

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Issued Date: 2019/12/26

Deciphered Date: yyyy/mm/dd

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

Sheet: 16 of 136

Rev: 0.3

# PCH GPIO(1/2)

**Others PU**

- VCC1R8\_SUS: R1652 1 2 1/20W 10K 5% 0201 -LID\_CLOSE\_R
- VCC3\_SUS: R1634 1 2 1/20W 10K 5% 0201 -PMC\_ALERT

**Core\_VID**

- CPUCORE\_AUX\_VID1: R1635 1 2 0.0201 SP
- PCHCORE\_VID1: R1636 1 2 0.0201 SP
- CPUCORE\_AUX\_VID0: R1637 1 2 0.0201 SP
- PCHCORE\_VID0: R1638 1 2 0.0201 SP

**HDA Signals**

- HDA\_SYNC\_R: R1617 1 2 1/20W 1K 5% 0201
- HDA\_RST\_R: C1605 1 2 2P 25V C.NPO 0201
- HDA\_BCLK: R1604 1 2 47P 25V J.NPO 0201

**For CNVi**

- BRI\_RSP\_CNVI: R1602 1 2 1/16W 20K 1% 0402
- RGI\_RSP\_CNVI: R1603 1 2 1/16W 20K 1% 0402

**GPU Control Pin**

- GPU\_RST: R1627 1 2 1/20W 10K 5% 0201
- TBTA\_HPD: R1631 1 2 0.0201 SP

**PLANARID**

PLANAR ID	3	2	1	0
R1623	R1624	R1625	R1626	
1	NA	NA	NA	
0	ASM	ASM	ASM	ASM

LEVEL	PLANARID[3..0]	CPU	PCH
PDV	-----	-----	-----
EVT	0001b	TBD	TBD
FVT	0010b	TBD	TBD
SIT	0011b	TBD	TBD
SVT			

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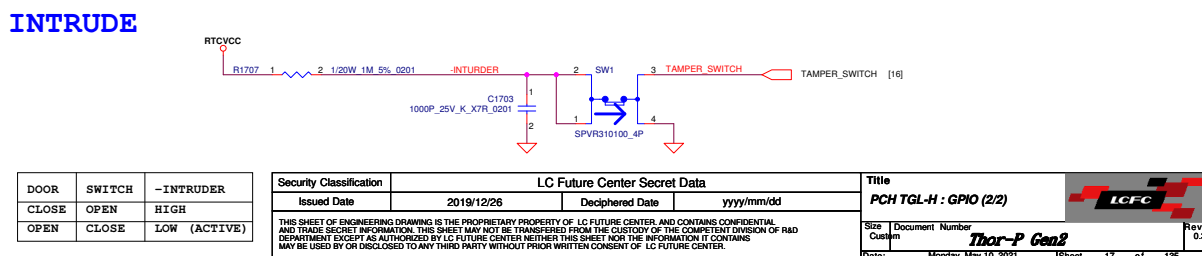
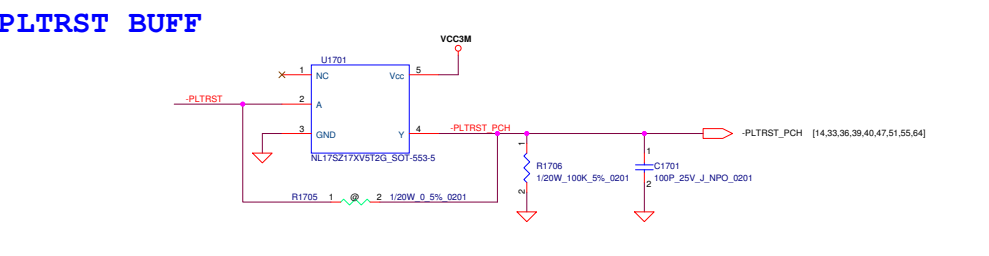
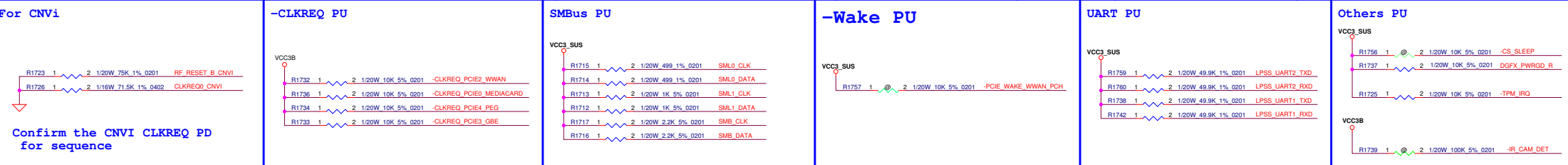
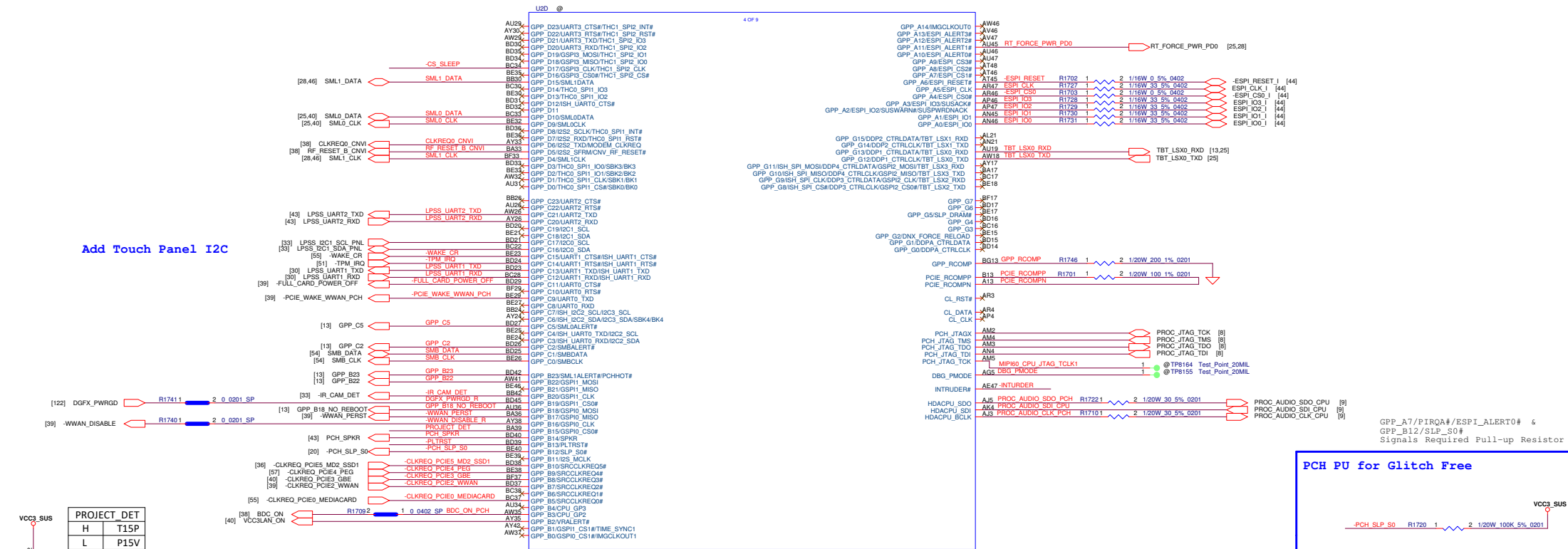
Document Number: Thor-P Gen2

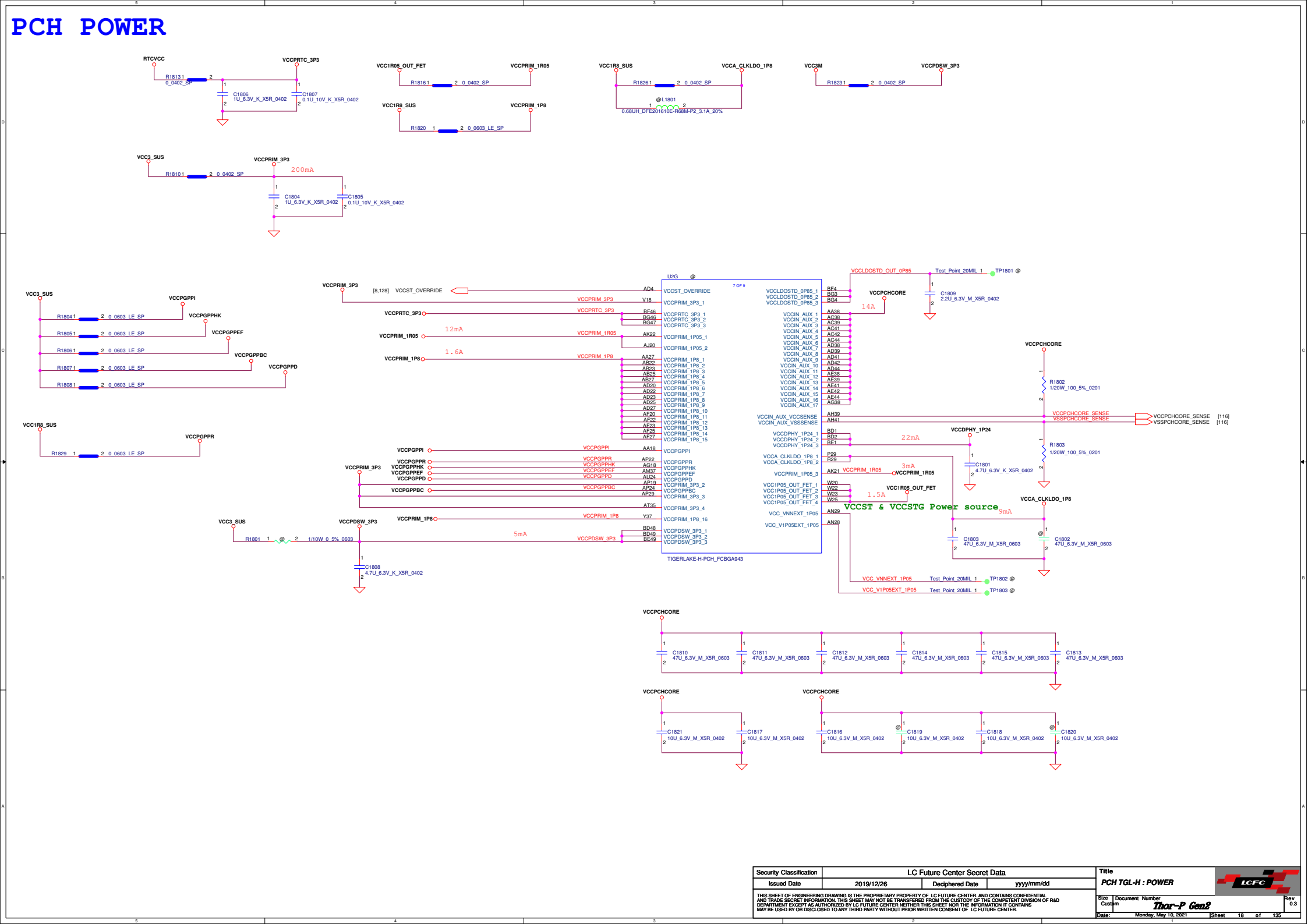
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Sheet: 16 of 136

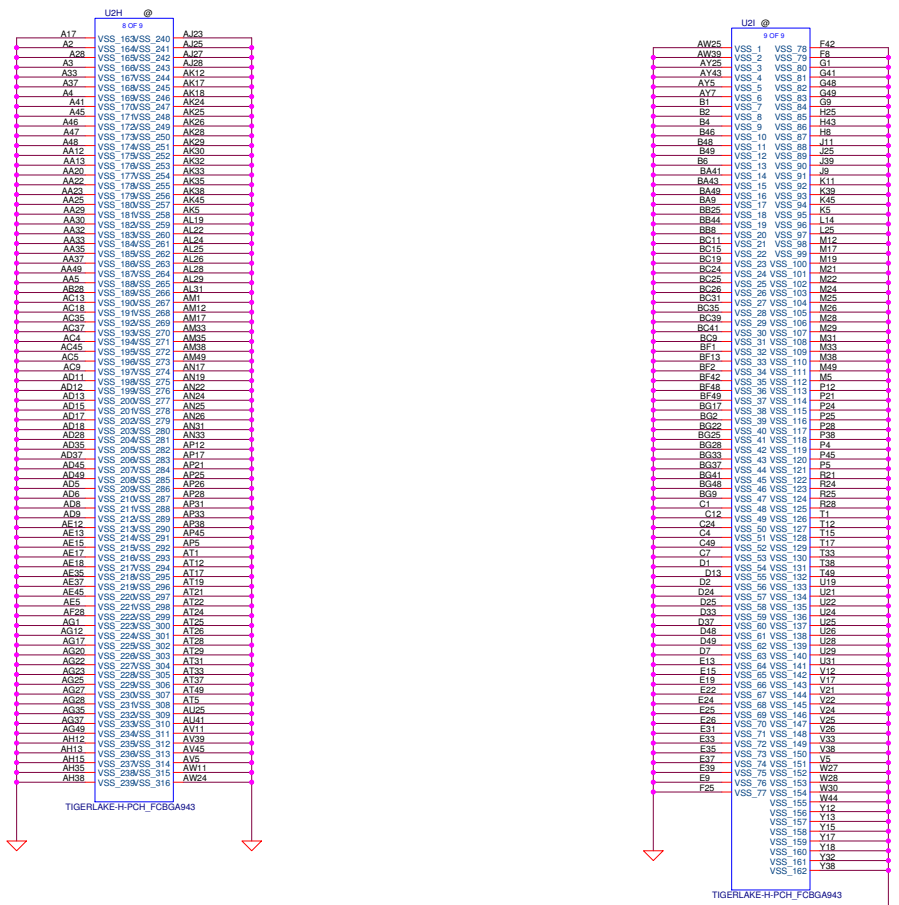
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PCH GPIO(2/2)

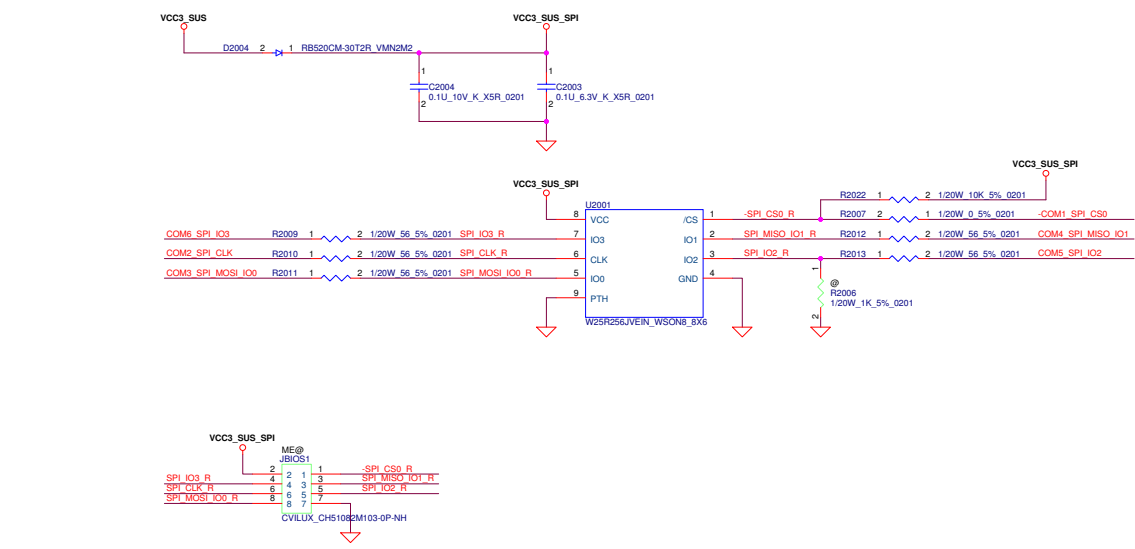


[illegible][illegible]

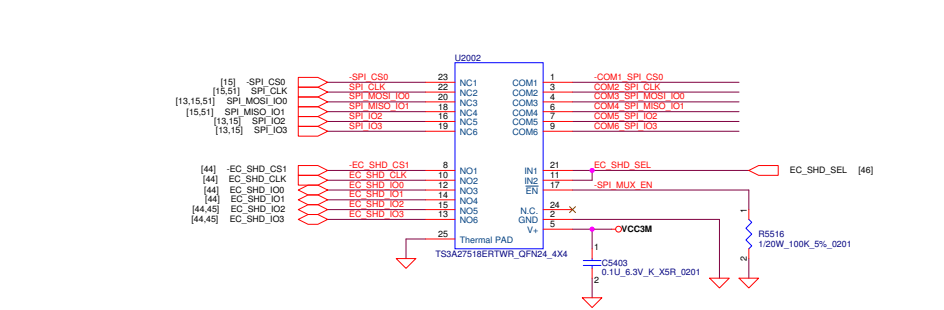
PCH GND



PCH SPI FLASH (Support RPMC)

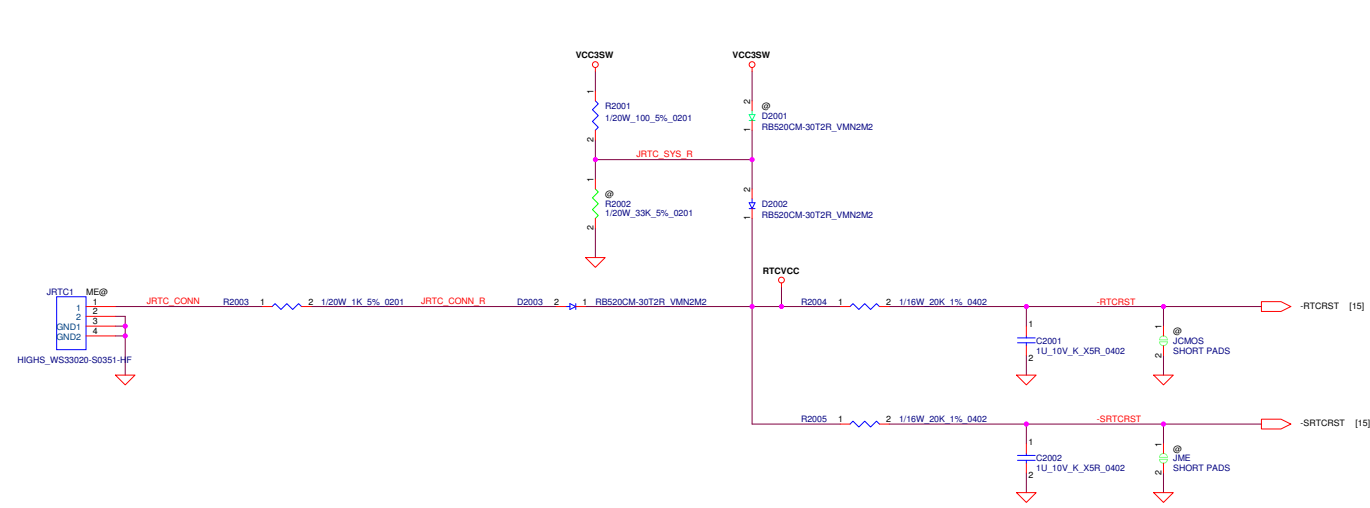


SPI Switch

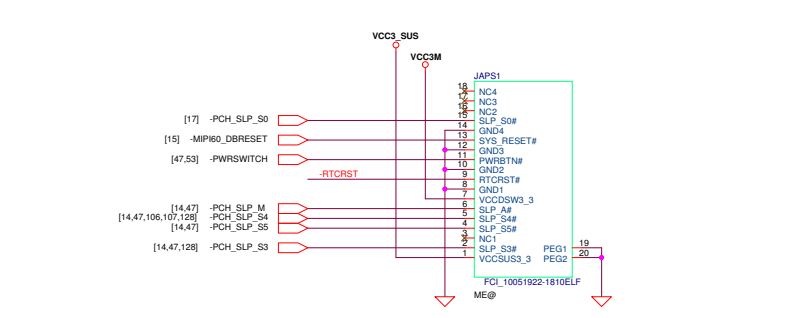


EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

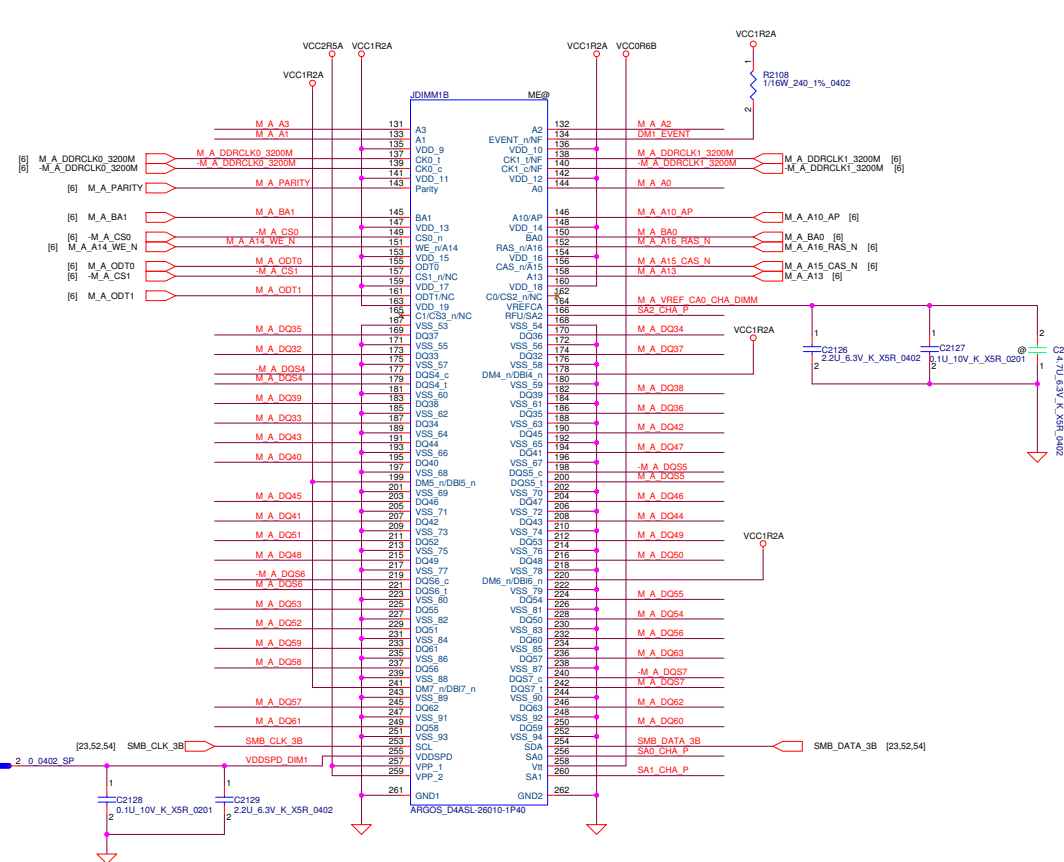
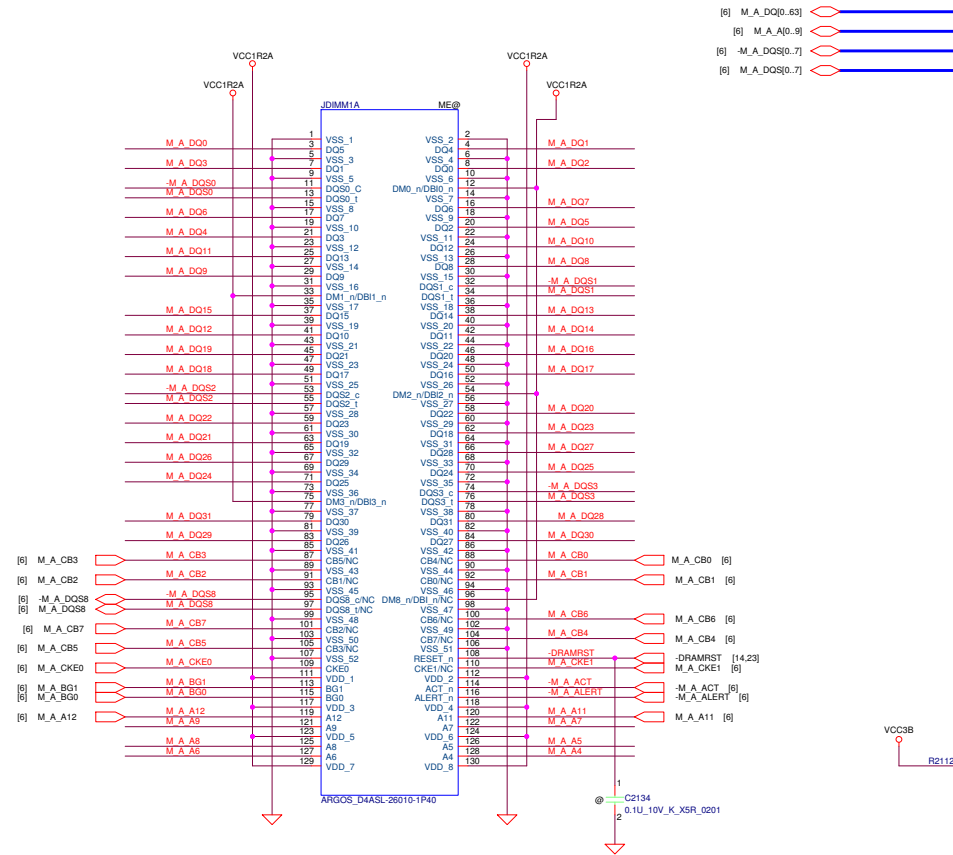
RTC



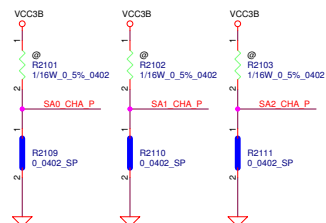
APS CONN



## DDR4 CH-A Parimary

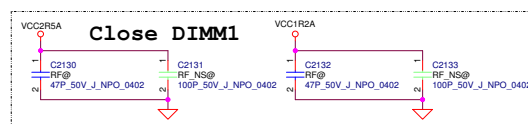
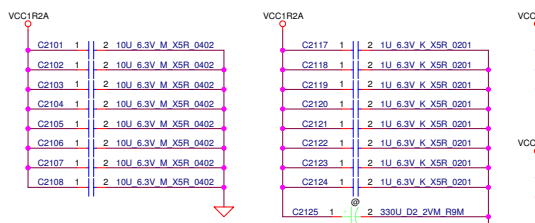


## SA0~2

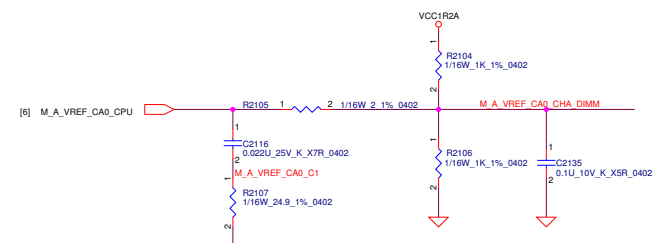



SPD Address = 0H

## SO-DIMM CAPs




## CHA\_VREF\_CA0



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Date:				Monday, May 10, 2021	Sheet	21 of 136	

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						<small>Custom</small>	<i>Thor-P Gen2</i>	
<small>Date:</small>						<small>Monday, May 10, 2021</small>		
<small>Sheet</small>						<small>22 of 135</small>		

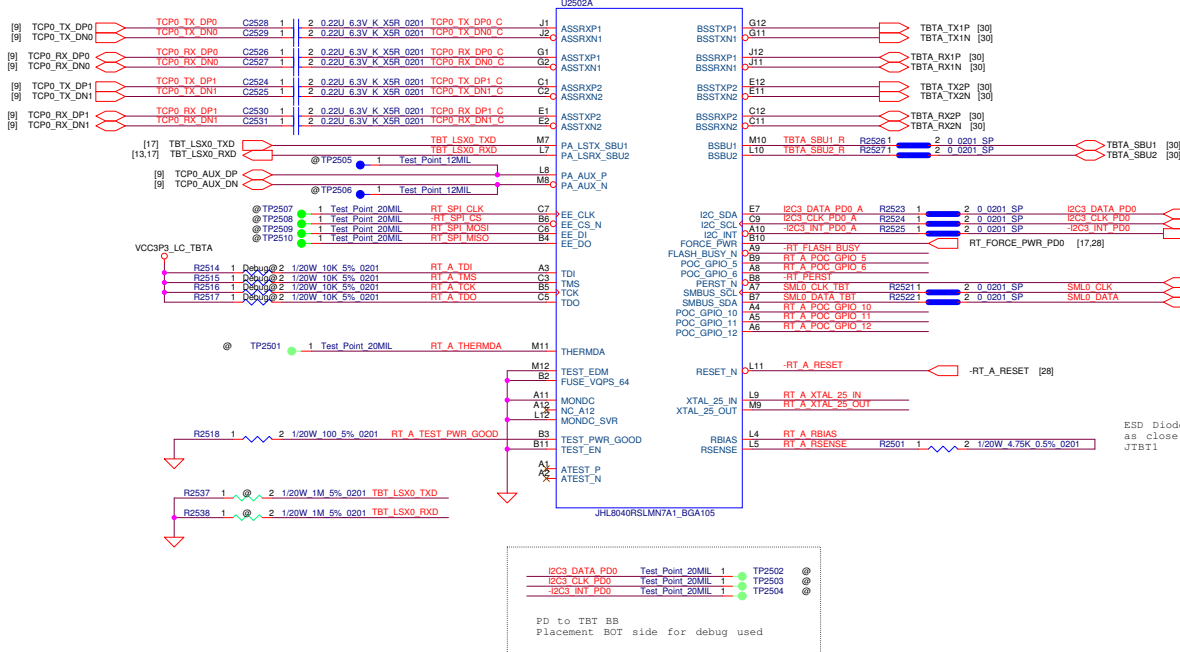




BLANK

Security Classification		LC Future Center Secret Data		Title		
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2019/12/26		yyyy/mm/dd		Size		Rev
				Document Number		
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				Date: Monday, May 10, 2021		
				Sheet 24 of 135		

TBT Re-timer A



TBT Re-timer A Strap in

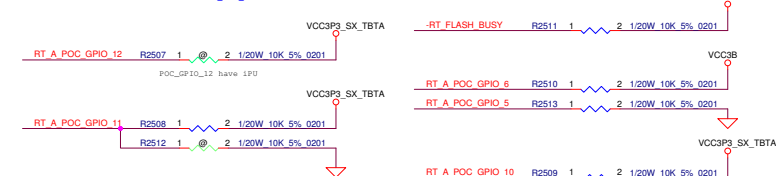


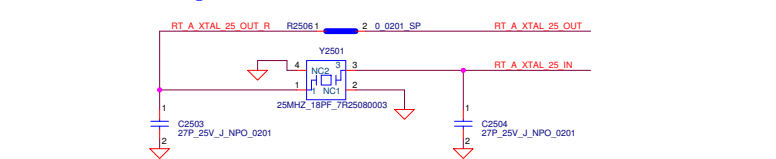
TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	Logic
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

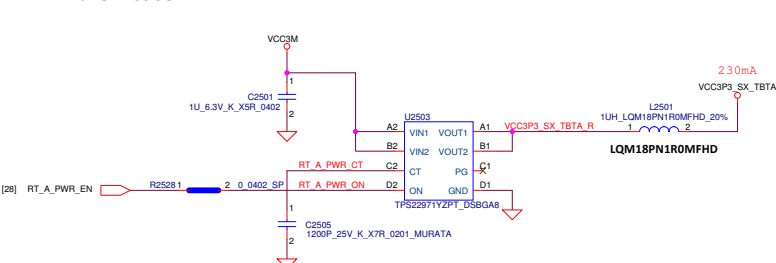
TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	Logic
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

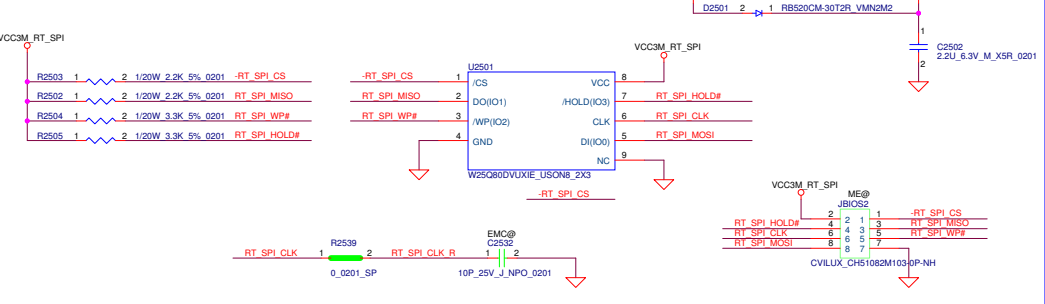
TBT Re-timer A Crystal



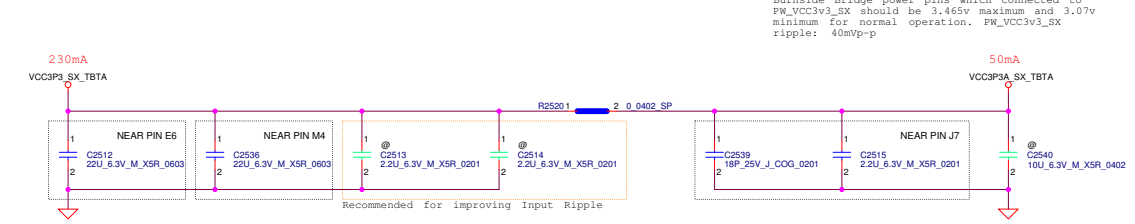
TBTA Power Gate




TBT Re-timer A&B SPI ROM




TBT Re-timer A PWR



BLANK

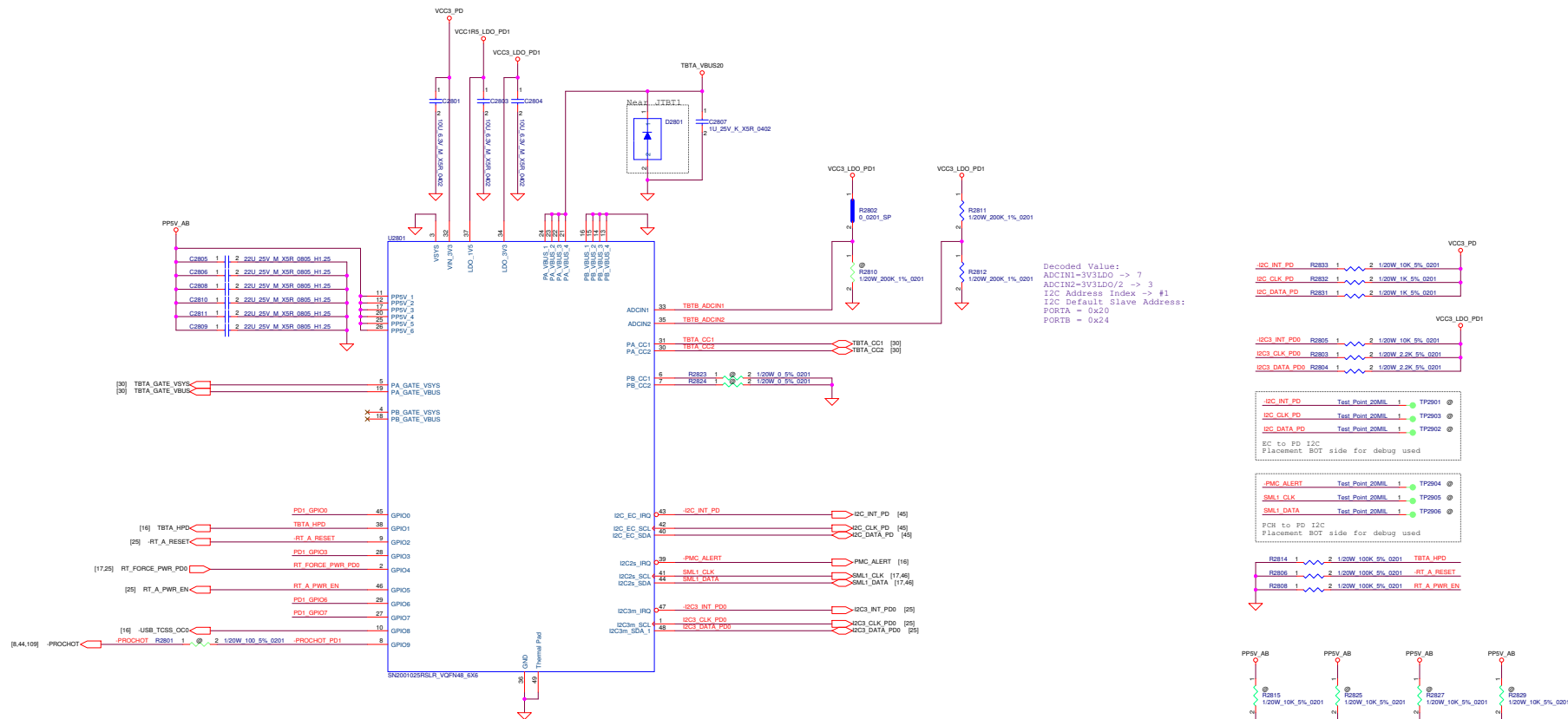
Security Classification		LC Future Center Secret Data		Title		
Issued Date		Deciphered Date		TBT RETIMER B		
2019/12/26		yyyy/mm/dd				
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Document Number		Raptor & Blackbird Gen2		0.3		
Date:		Monday, May 10, 2021		Sheet		26 of 133

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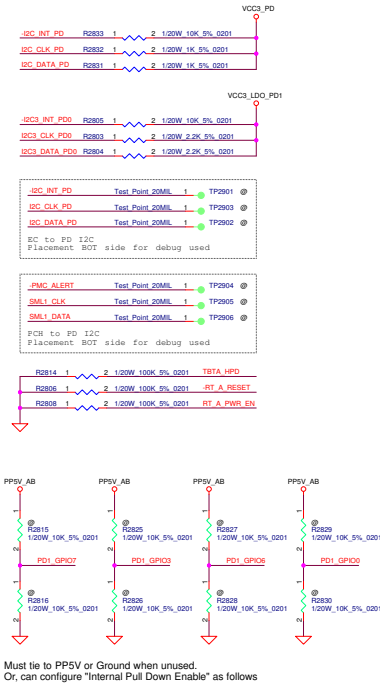
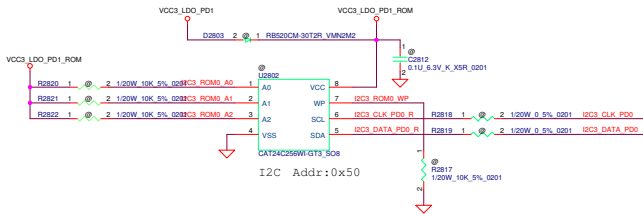
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	USB-C X-Bar	
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				Document Number	
				Date: Monday, May 10, 2021	Sheet 27 of 133

Raptor & Blackbird Gen2


PD Controller-1 TI65994



TBT PD I2C ROM




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Issued Date		Deciphered Date		Type-C PD Controller-2			
2019/12/26		yyyy/mm/dd					
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				Custom		0.3	
Date: Monday, May 10, 2021				Sheet 29 of 135			



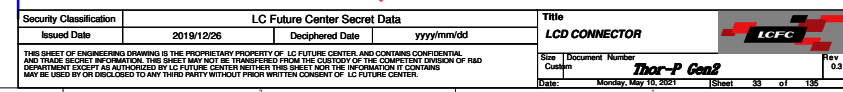


BLANK

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Issued Date		Deciphered Date		USB TYPE-C CONNECTOR					
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						<small>Date:</small>	<small>Monday, May 10, 2021</small>		

BLANK

## CAMERA/TOUCH



HDMI2.0 Retimer PS8409

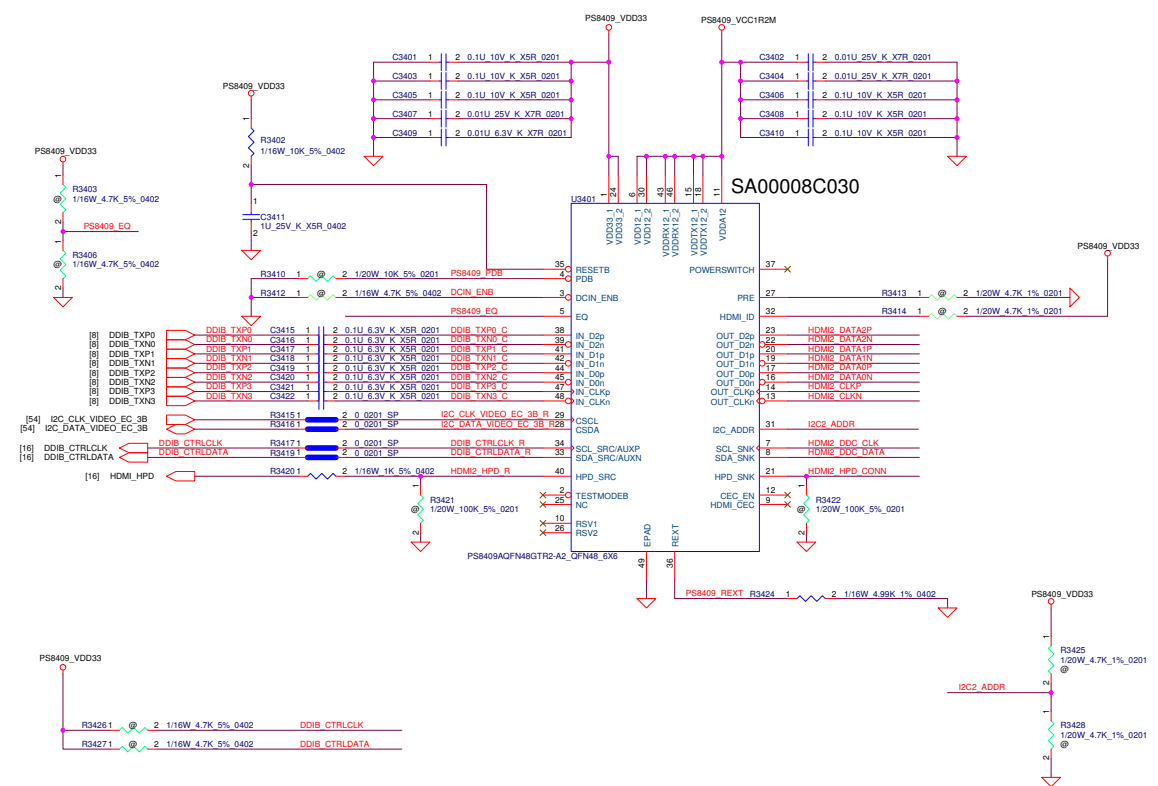
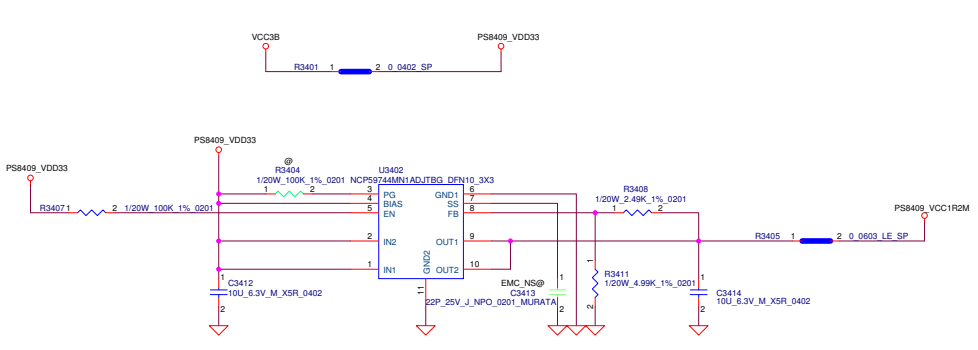


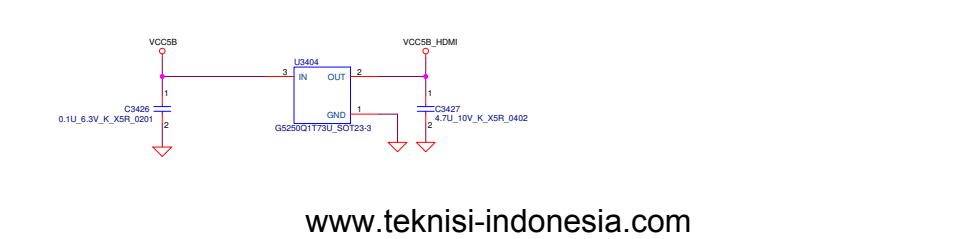
TABLE I2C Address  
Retimer internally pulled down at ~150KΩ .

I2C_ADDR	
LOW	0x10-0x2F ← Logic
HIGH	0x90-0x9F; 0xD0-0xDF

PS8409 PWR

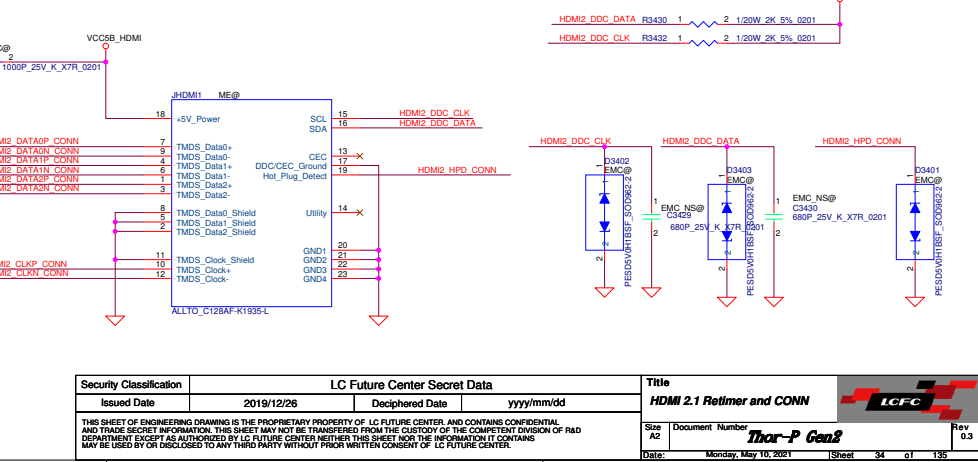
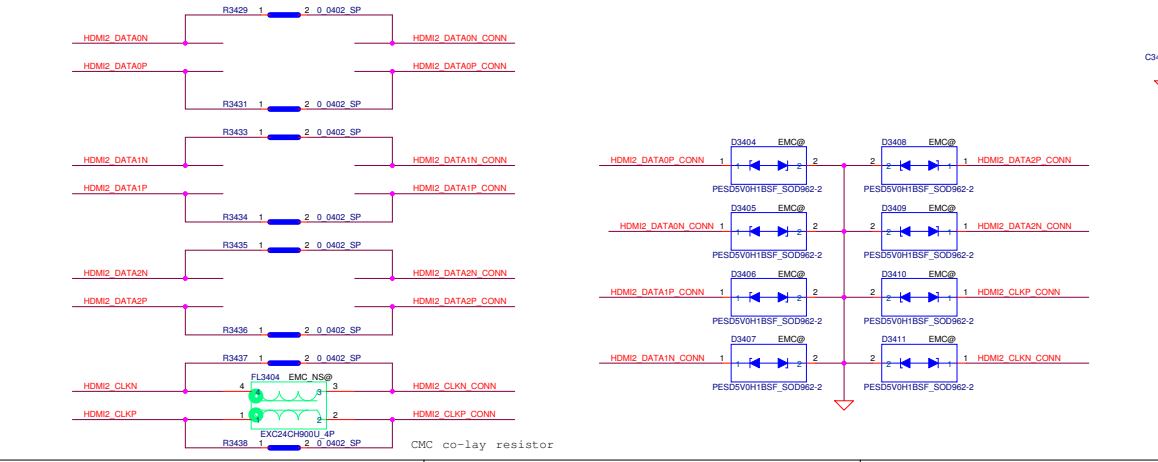


HDMI CONN PWR




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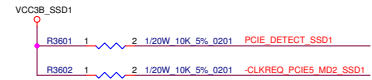
HDMI 2.0 CONN Meowth\_LCFC\_EC023/65



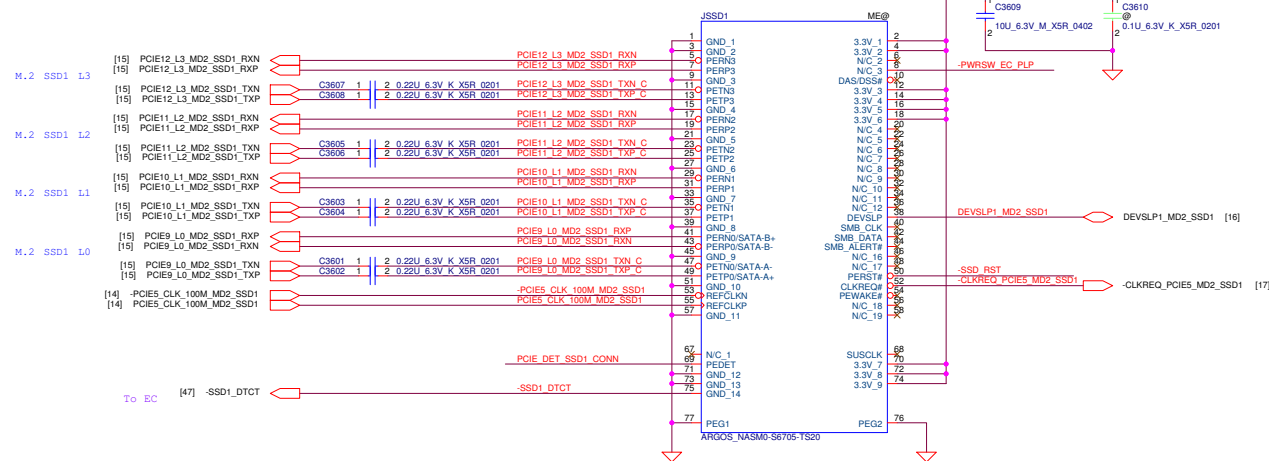
BLANK

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Issued Date		2015/07/16	Deciphered Date	2016/01/16	BLANK	
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Date: Monday, May 10, 2021						Sheet 35 of 135

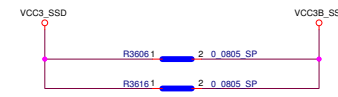
M.2 SSD Slot1



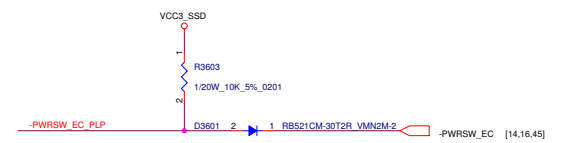
M.2 SSD slot 1  
Type-M 2280



SSD Slot1 PWR



PLP for NVMe SSD



SATA/PCIE PEDET

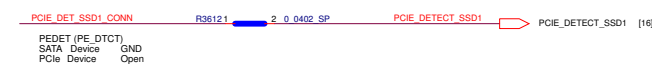
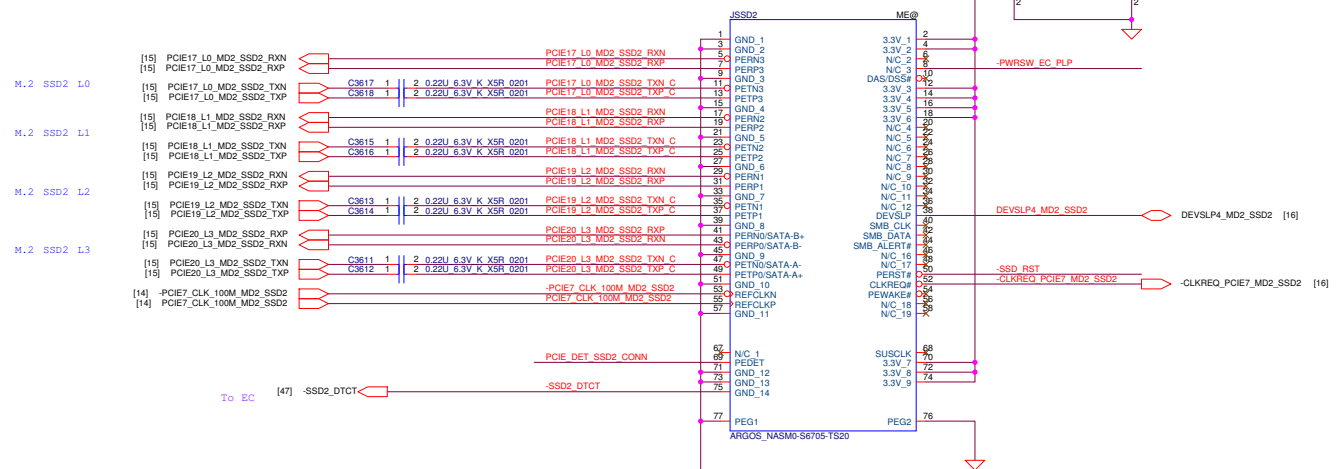


TABLE	
-PCIE_DETECT_SSD1	Device
High	PCIe SSD
LOW	SATA SSD

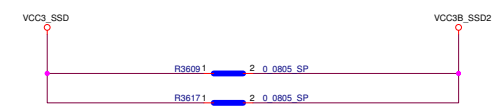
M.2 SSD Slot2



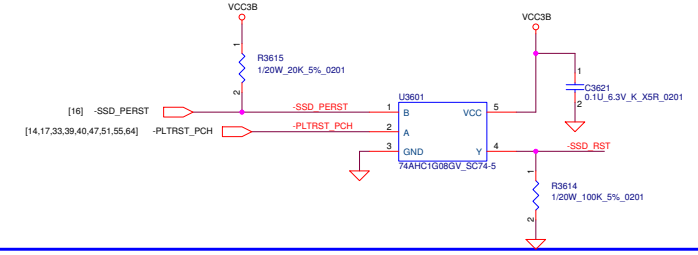
M.2 SSD slot 2  
Type-M 2280



SSD Slot2 PWR



SSD1&2 RTD3




SATA/PCIE PEDET



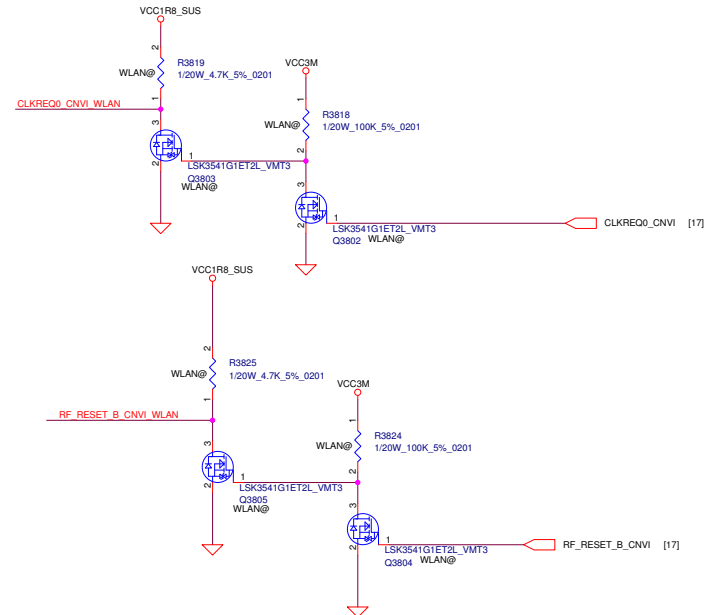
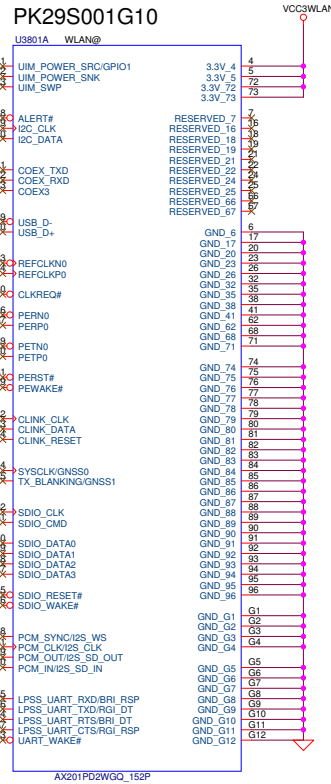
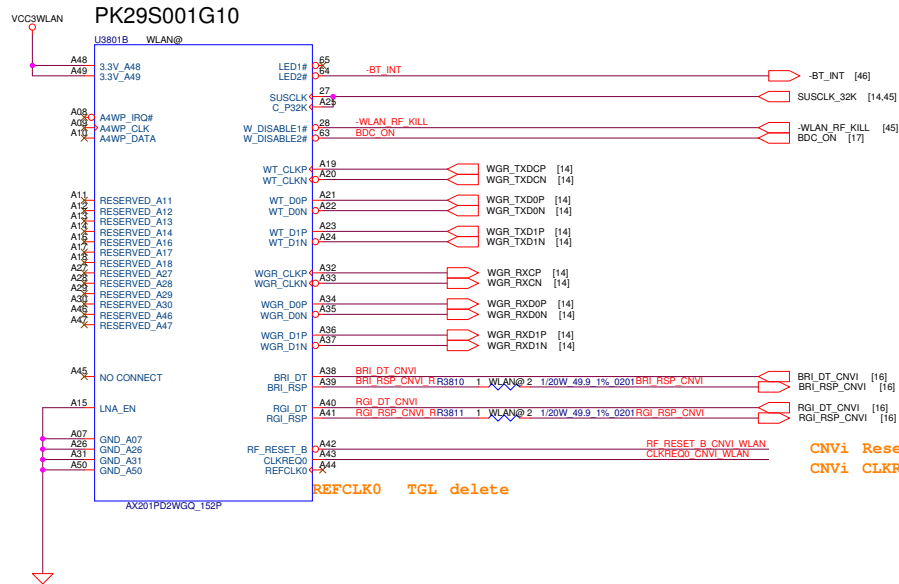
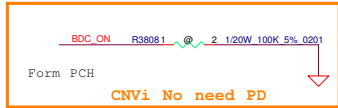
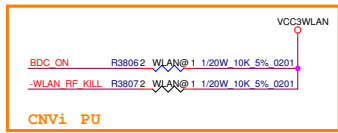
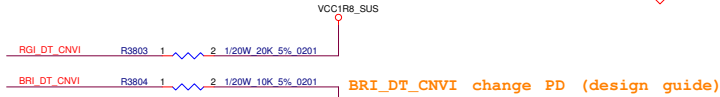
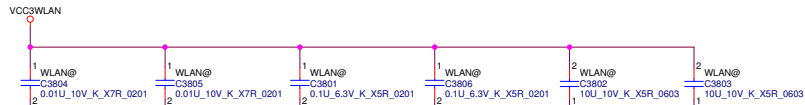
TABLE	
-PCIE_DETECT_SSD2	Device
High	SATA SSD
LOW	PCIe SSD



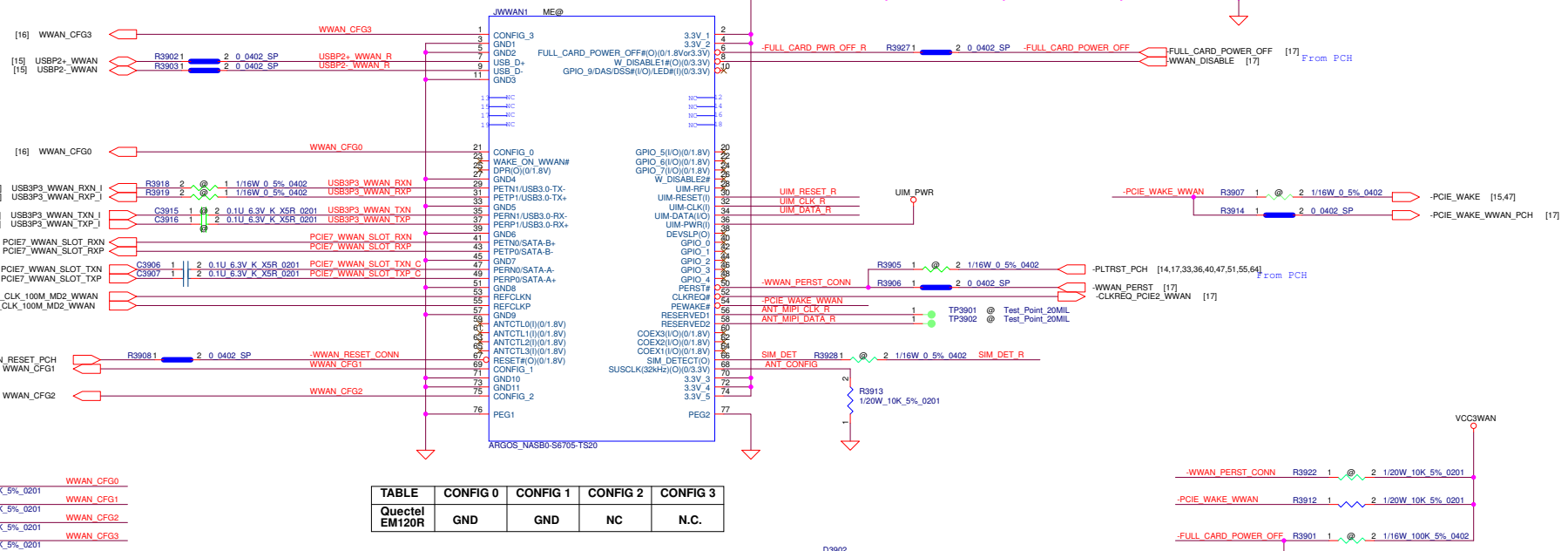
5					4					3					2					1										
D																														
C																														
B																														
A																														
Security Classification					LC Future Center Secret Data										Title															
Issued Date					2019/12/26					Deciphered Date					yyyy/mm/dd										M.2 NVMe Gen4 SSD SLOT_3					
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																				C				Thor-P Gen2					0.3	
Date:					Monday, May 10, 2021										Sheet					37 of 135										

# WLAN Harrison Peak 2

On board WLAN\_1216

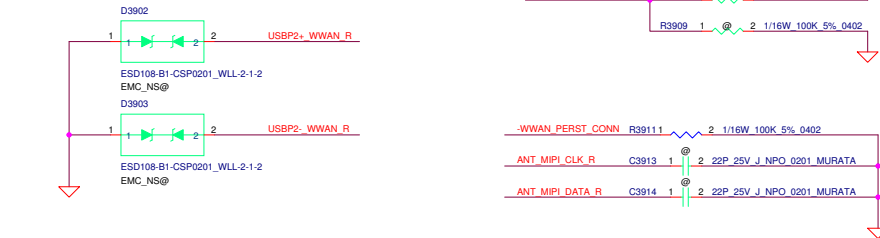
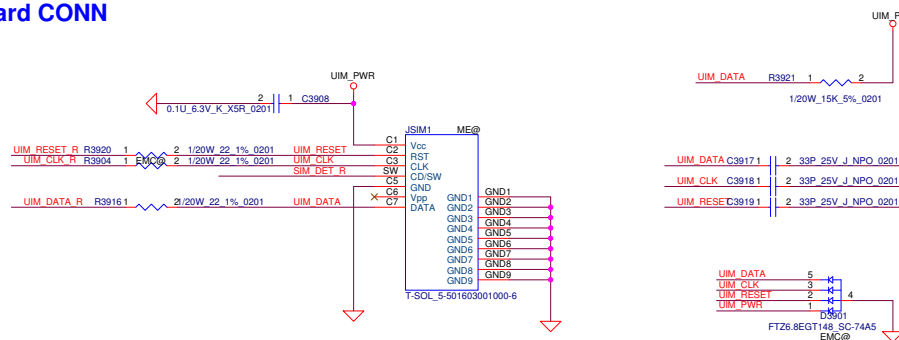



M.2 Socket 2 (Key-B) for 3042 S3 WWAN  
H=2.00mm Connector



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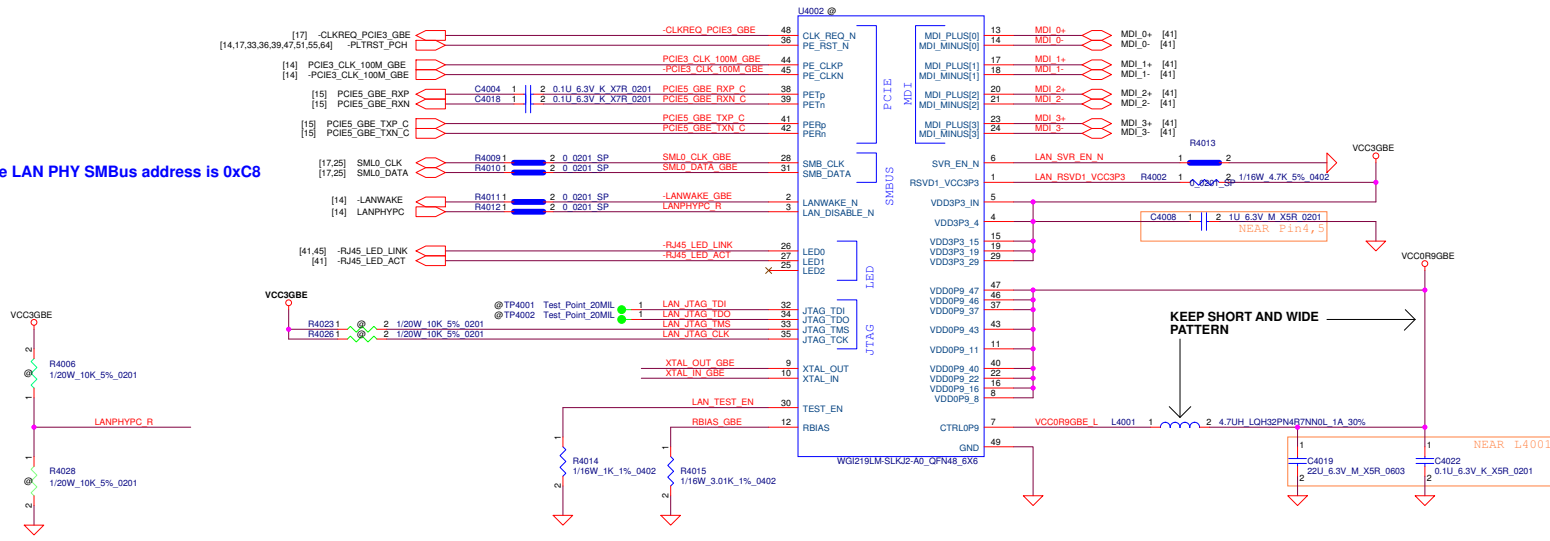
## SIM Card CONN



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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd		M.2 WWAN CARD SLOT				
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Date:		Monday, May 10, 2021		Sheet		39 of		135	

# Intel LAN I219

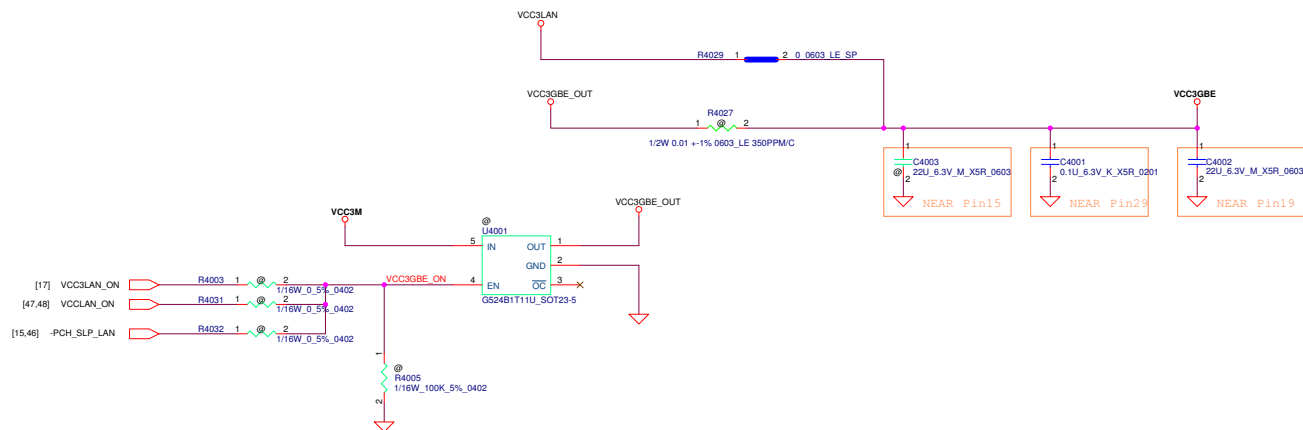
The LAN PHY SMBus address is 0xC8



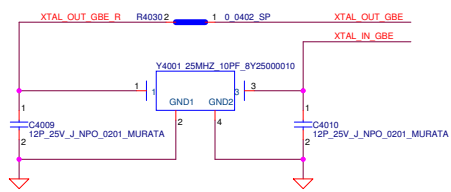
## LAN Others PU



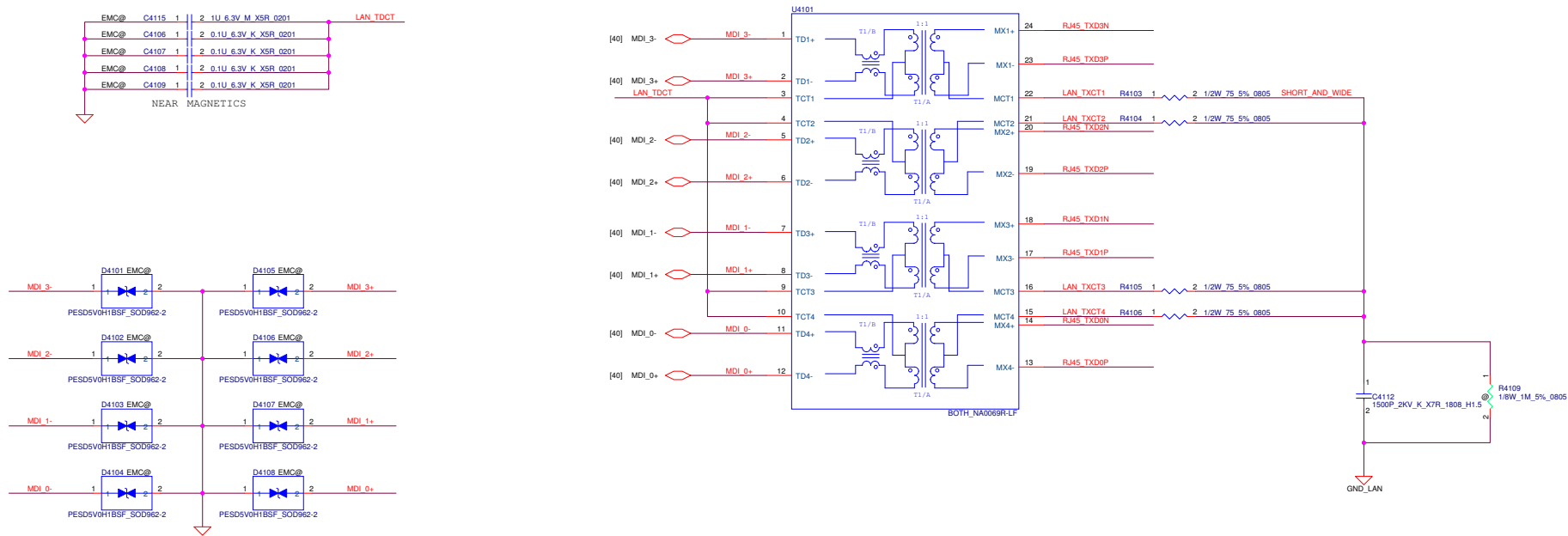
## LAN PWR



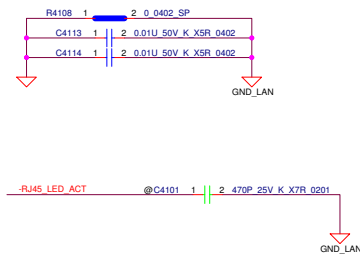
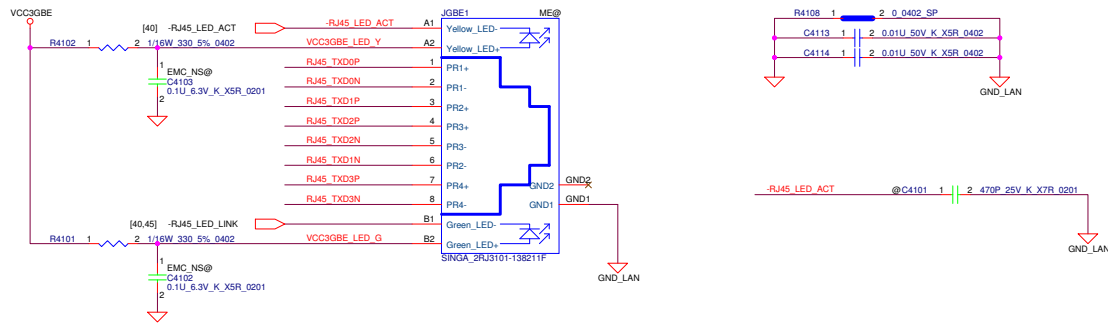
## LAN Crystal




# 1G Transformer



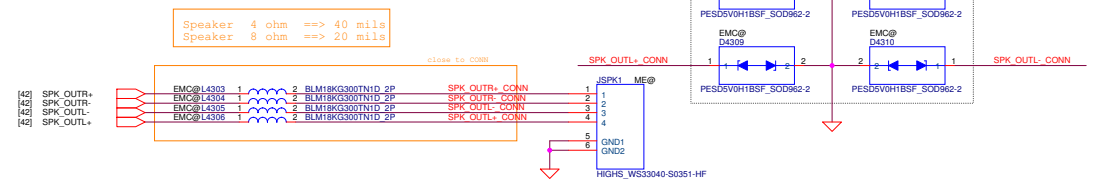
# RJ45 CONN



## AUDIO JACK SENSE

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Date				Monday, May 15, 2021		Sheet 42 of 135	

**SPEAKER**



**NEAR EXT MIC CONN**

[42] MIC2\_VREF0\_R → MIC2\_VREF0\_R → R4308 (1/20W, 2.2K, 5%, 0201) → R4309.1 (2, 0.0201 SP) → MIC\_SLEEVE → MIC\_SLEEVE\_CODEC [42]

[42] MIC2\_VREF0\_L → MIC2\_VREF0\_L → R4310 (1/20W, 2.2K, 5%, 0201) → R4311.1 (2, 0.0201 SP) → MIC\_SLEEVE → MIC\_SLEEVE\_CODEC [42]

MIC\_SLEEVE → R4312.1 (2, 0.0402 SP) → MIC\_SLEEVE\_CODEC [42]

MIC\_RING2 → R4315.1 (2, 0.0402 SP) → MIC\_RING2\_CODEC [42]

EMC Ⓢ

C4305 (0.01uF, 25V, K, X7R, 0402) → R4314.1 (2, 0.0402 SP) → AGND

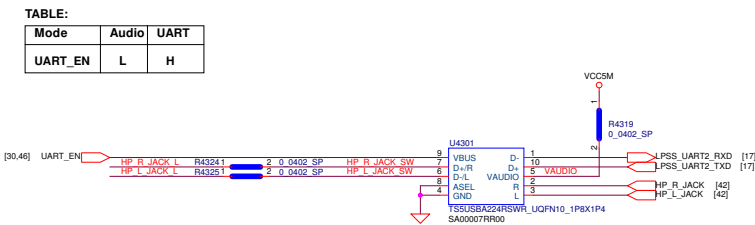
R4313 (1/20W, 0.5%, 0201) → AGND

R4316 (1/20W, 0.5%, 0201) → AGND

C4304 (1000pF, 25V, K, X7R, 0201) → AGND

C4306 (1000pF, 25V, K, X7R, 0201) → AGND

# AUDIO DEBUG PORT



Mode	Audio	UART
UART_EN	L	H

# NPCX997 (1/3)

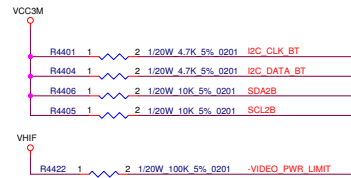
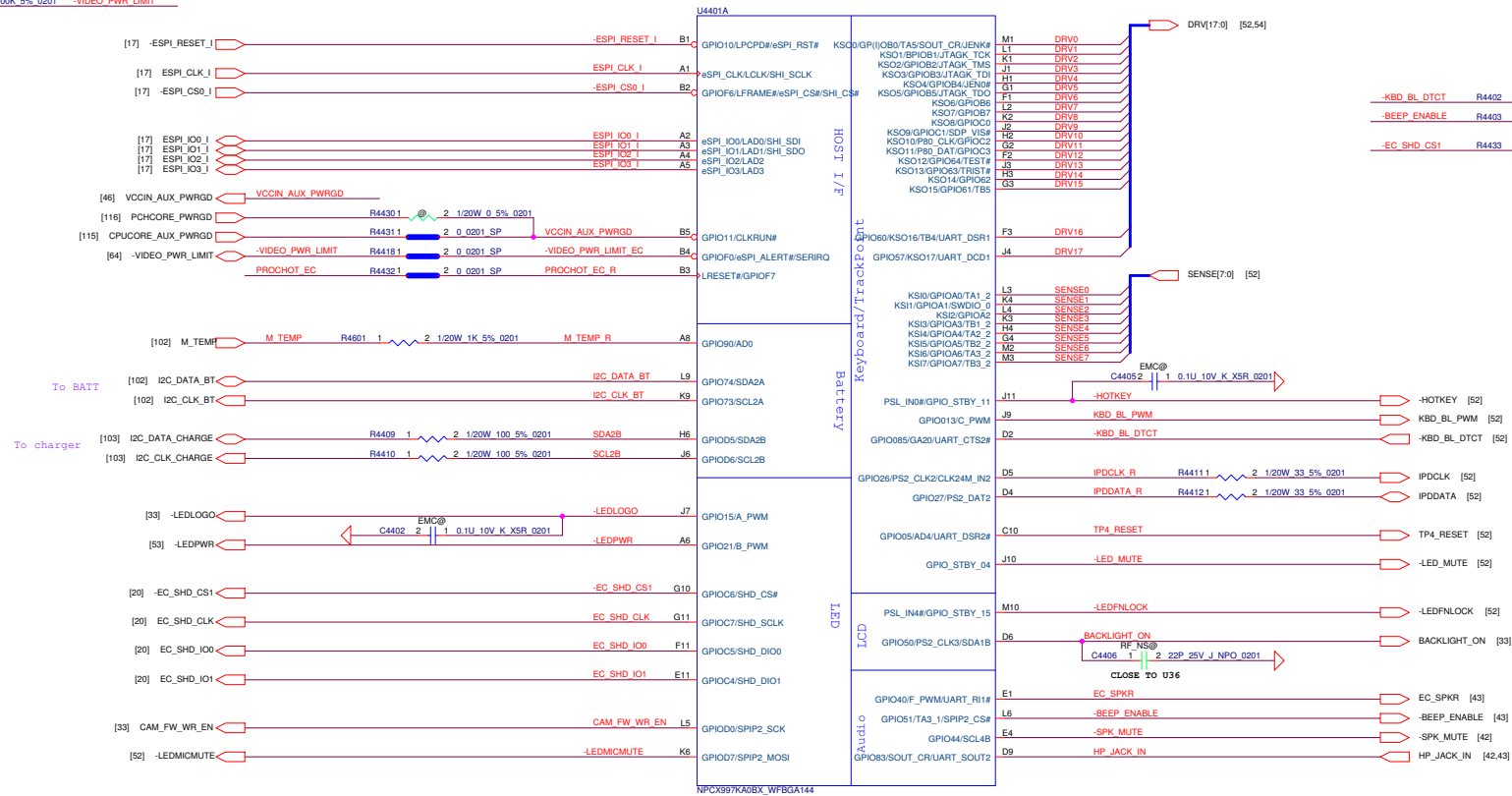


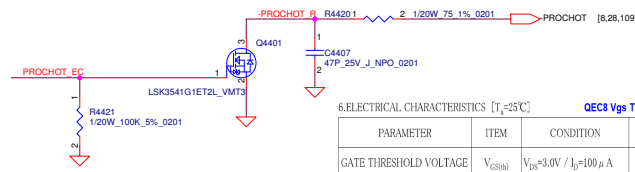
TABLE : Functional Strap

JEN1#/KSO0 (JTAG 1 Select)	
OPEN	JTAG K is disabled
LOW	JTAG K is selected

← LOGIC



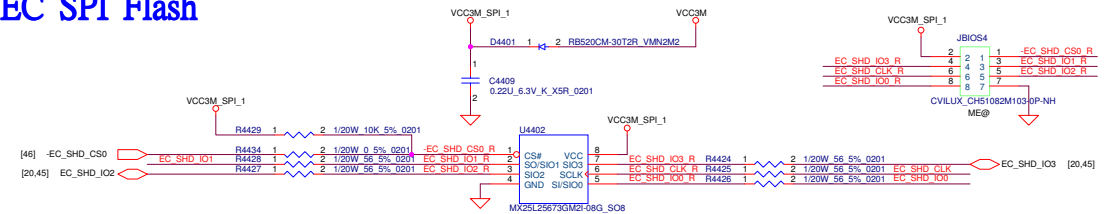
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6.ELECTRICAL CHARACTERISTICS [ $T_A=25^{\circ}\text{C}$ ]

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
GATE THRESHOLD VOLTAGE	$V_{GS(th)}$	$V_{DS}=3.0V / I_D=100\mu A$	0.8V	-	1.5V

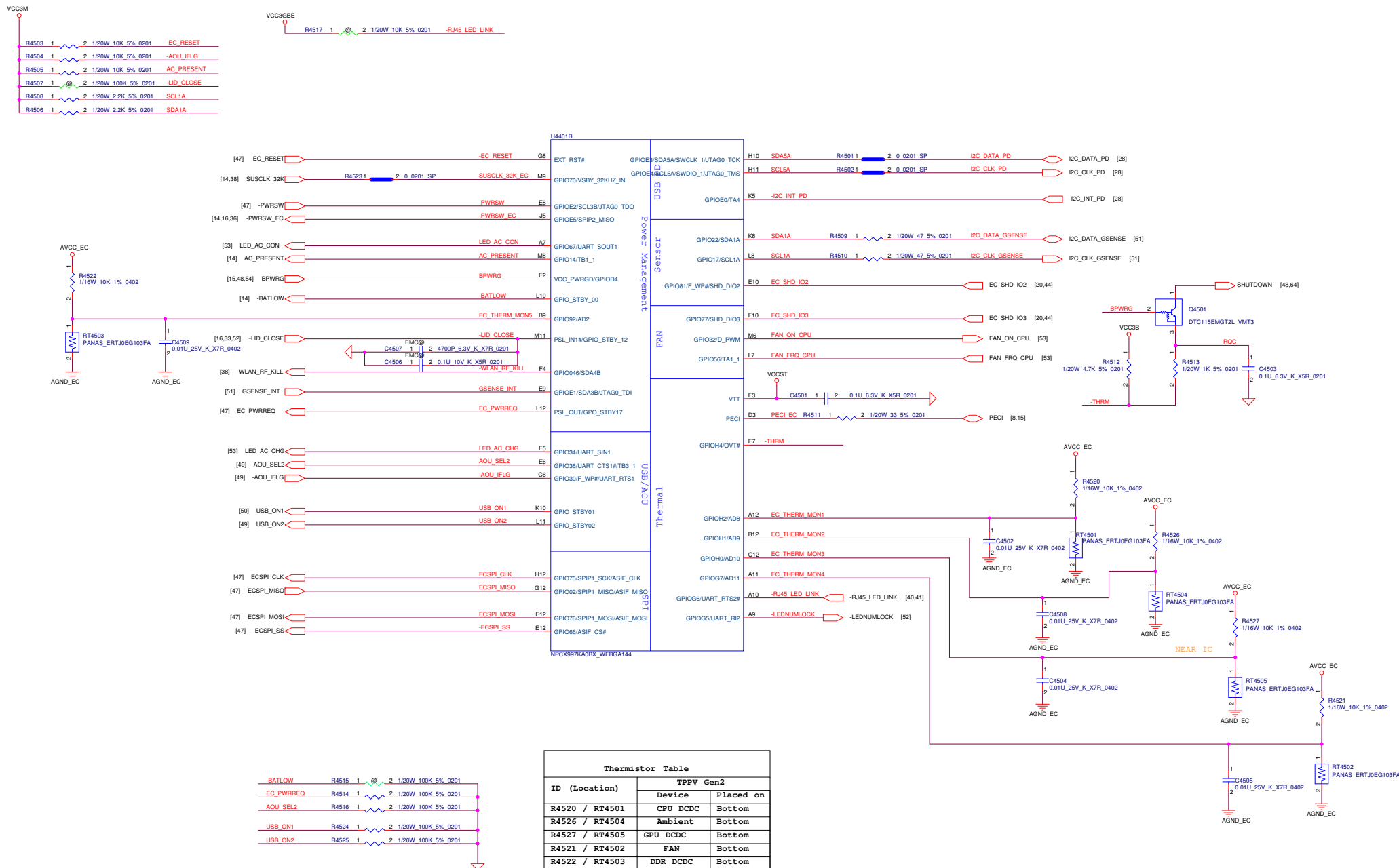
## EC SPI Flash



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					Rev 0.3 Sheet 44 of 135

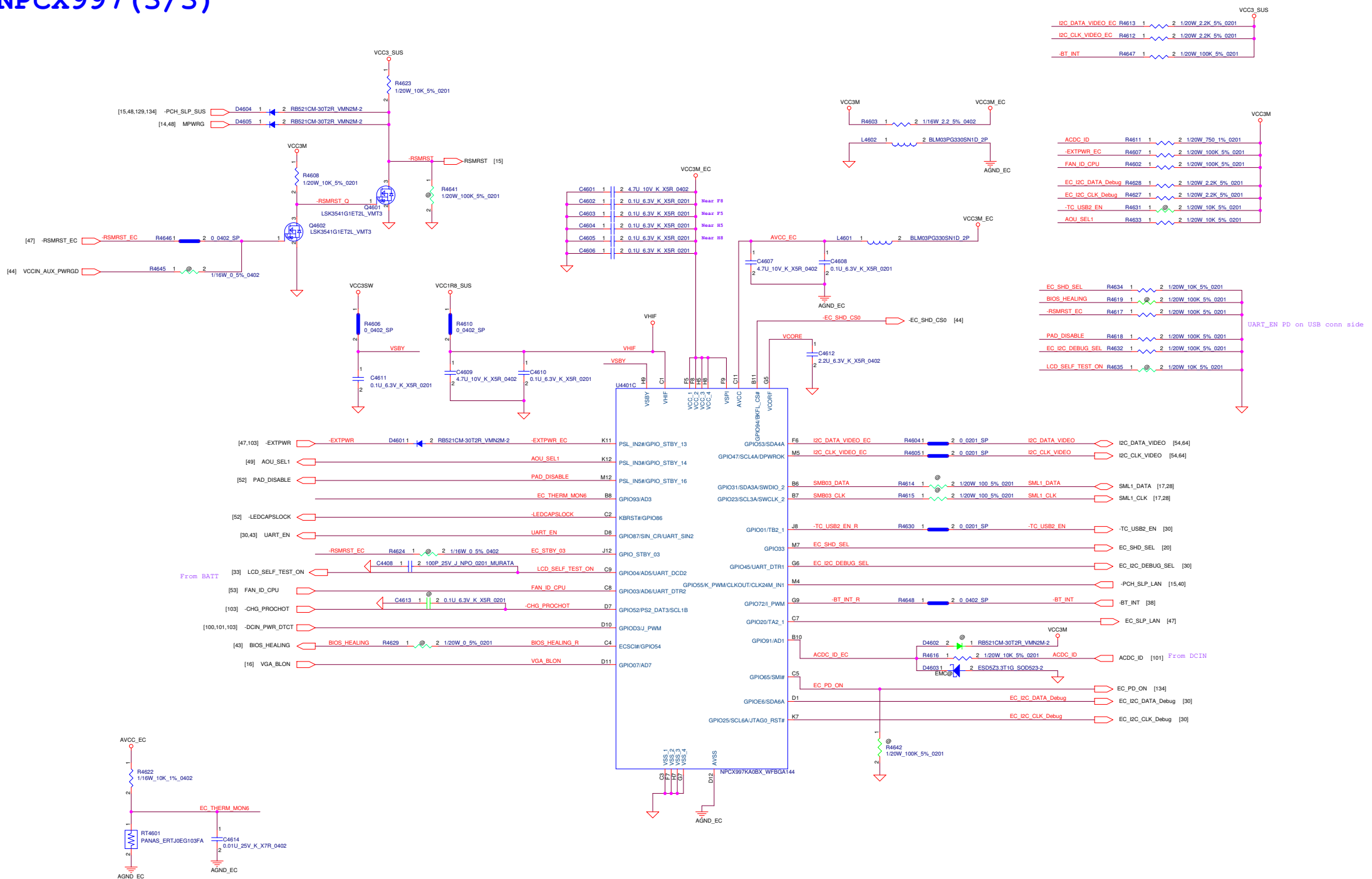





## NPCX997 (2/3)



Thermistor Table		
ID (Location)	TPPV Gen2	
	Device	Placed on
R4500 / RT4501	CPU DCDC	Bottom
R4526 / RT4504	Ambient	Bottom
R4527 / RT4505	GPU DCDC	Bottom
R4521 / RT4502	FAN	Bottom
R4522 / RT4503	DDR DCDC	Bottom
R4622 / RT4601	SSD	Bottom

## NPCX997 (3/3)



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				Sheet	46	of 136

**THINK ENGINE**

Rohm Think Engine-2 Short term solution

AND LOGIC. Once -PCH\_SLP\_S3 is de-asserted VCCST\_PWRGD and IMVP VR\_ON should be de-asserted in <= 1 usec. These are tCPU28 and tPLT17 defined in Intel SKL-H PDG. (CT\_20141216)

From EC & CHARGER

From EC/ PWR IC/Tunderbolt

These are device tamper detection pins. If storage is detached, BIOS will not automatically send password to storage.

BD4178AGSW-ZE2\_BGA080W080A80

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Issued Date: 2019/12/26

Deciphered Date: yyyy/mm/dd

Title: THINK ENGINE 2(1/2)

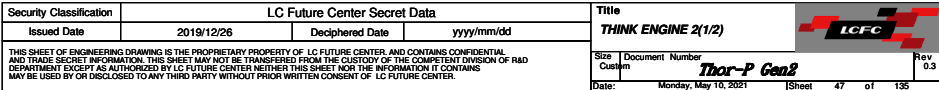
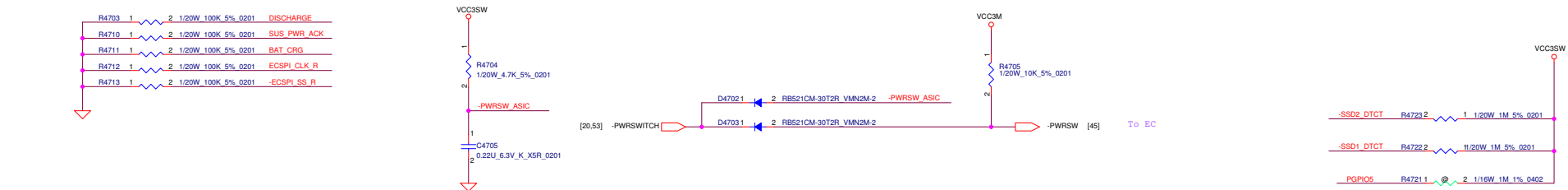
Size: 11.00mm

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

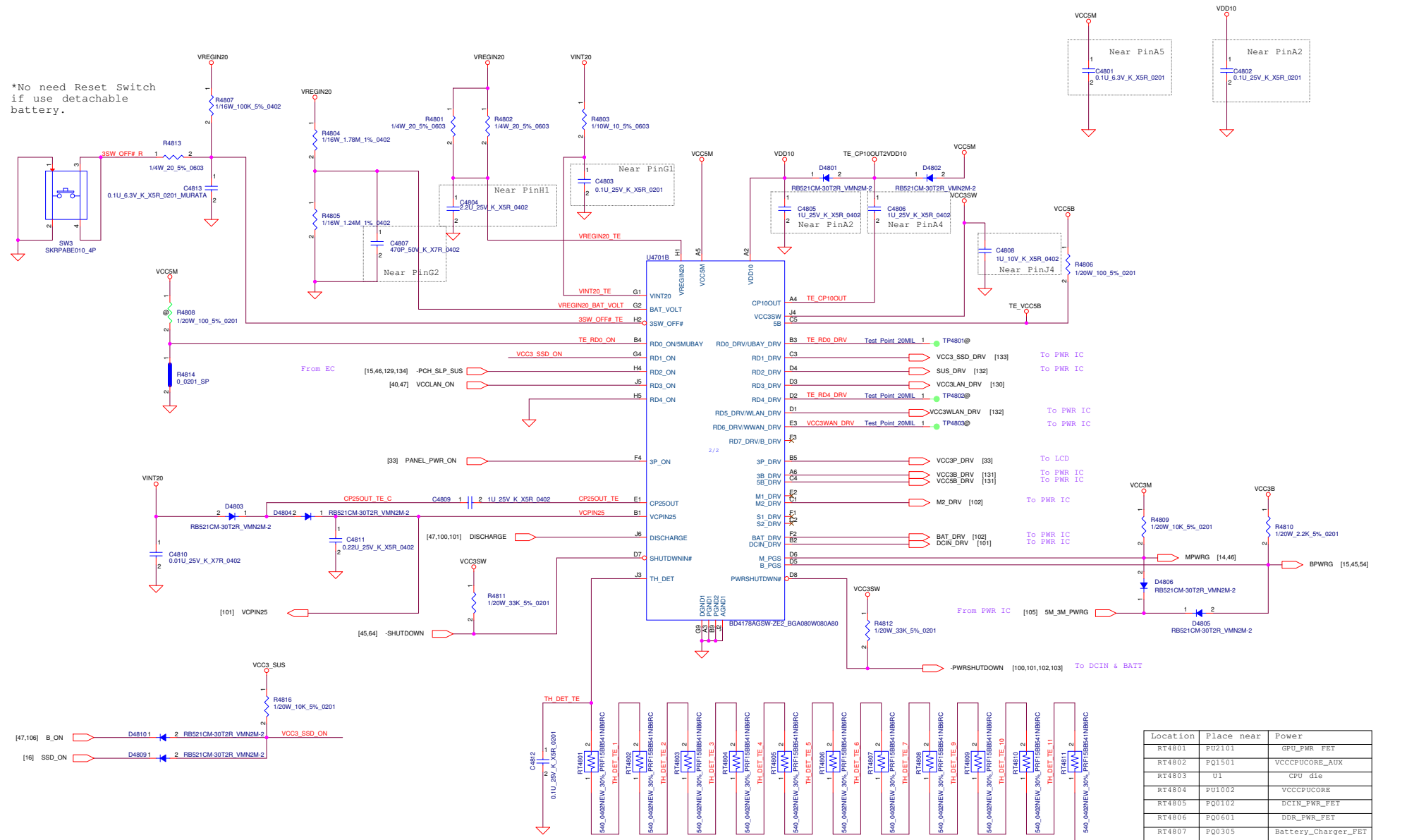
Sheet: 47 of 135

Rev: 0.3



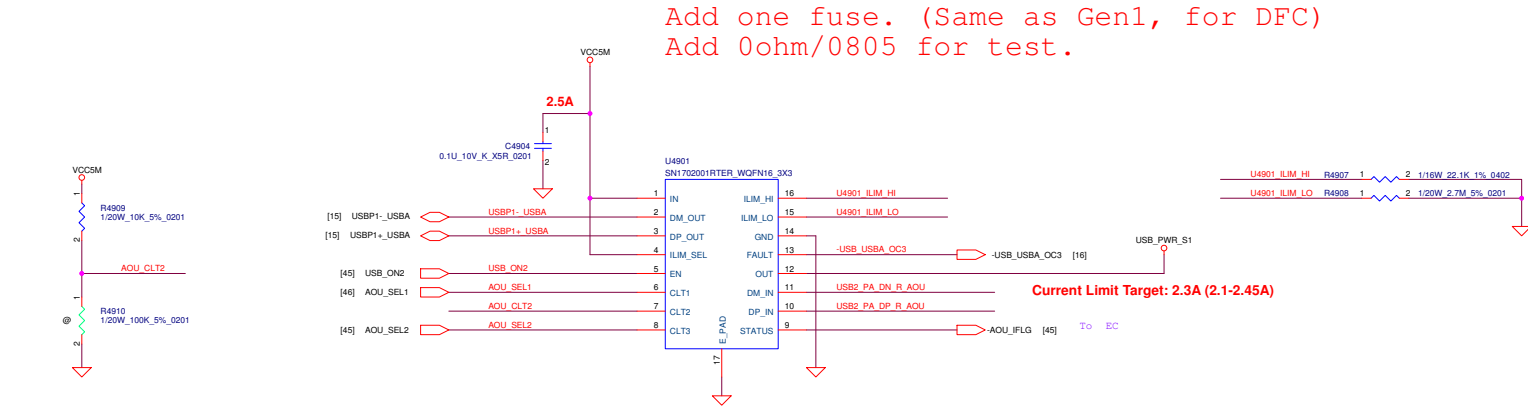
THINK ENGINE

\*No need Reset Switch  
if use detachable  
battery.

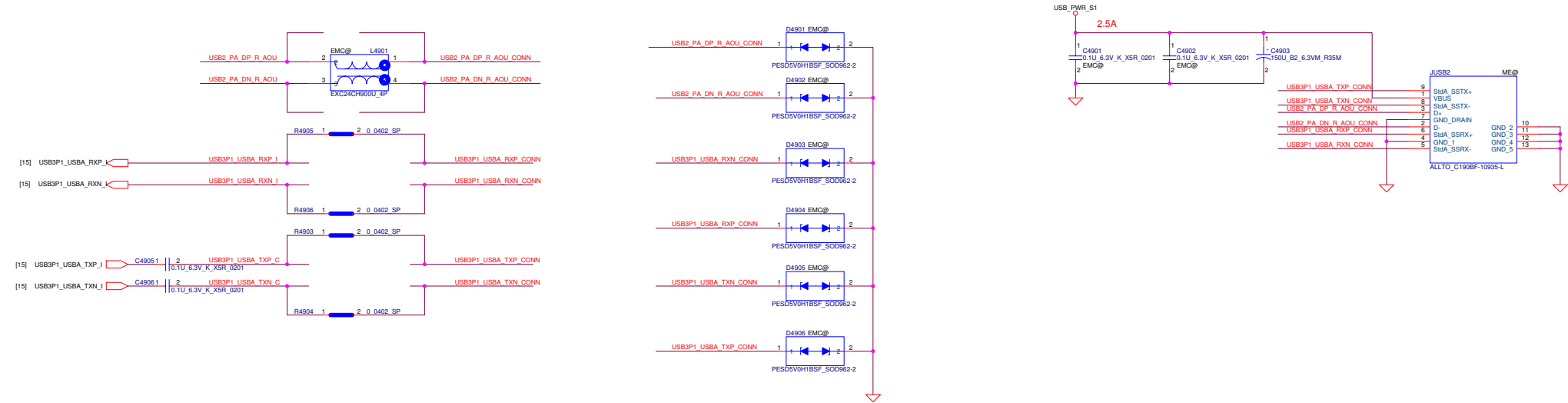


Location	Place near	Power
RT4801	P02101	GPU_PWR_FET
RT4802	P01501	VCCCPUCORE_AUX
RT4803	U1	CPU die
RT4804	P01002	VCCCPUCORE
RT4805	PQ0102	DCIN_PWR_FET
RT4806	PQ0501	DDR_PWR_FET
RT4807	PQ0305	Battery_Charger_FET
RT4808	PQ0504	VCC5M_PWR_FET
RT4809	PQ0202	M_BAT_PWR_FET
RT4810	PQ0506	VCC3M_PWR_FET
RT4811	PQ1601	VCCPCHCORE

USB AOU



USB Type-A Port A CONN



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## USB3.1 CONN

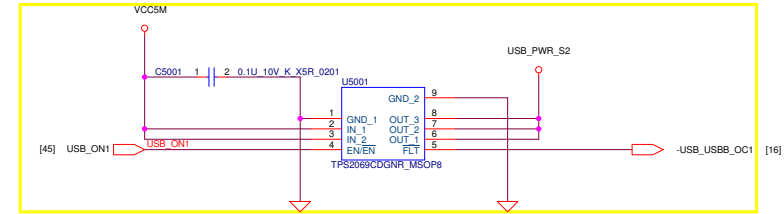
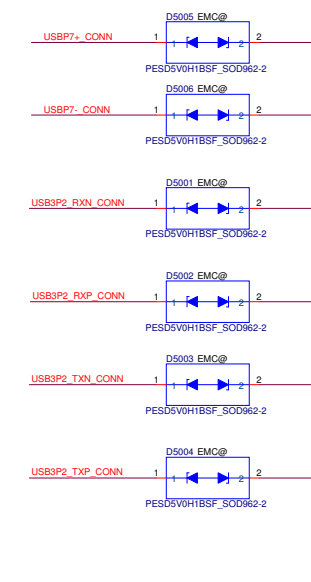
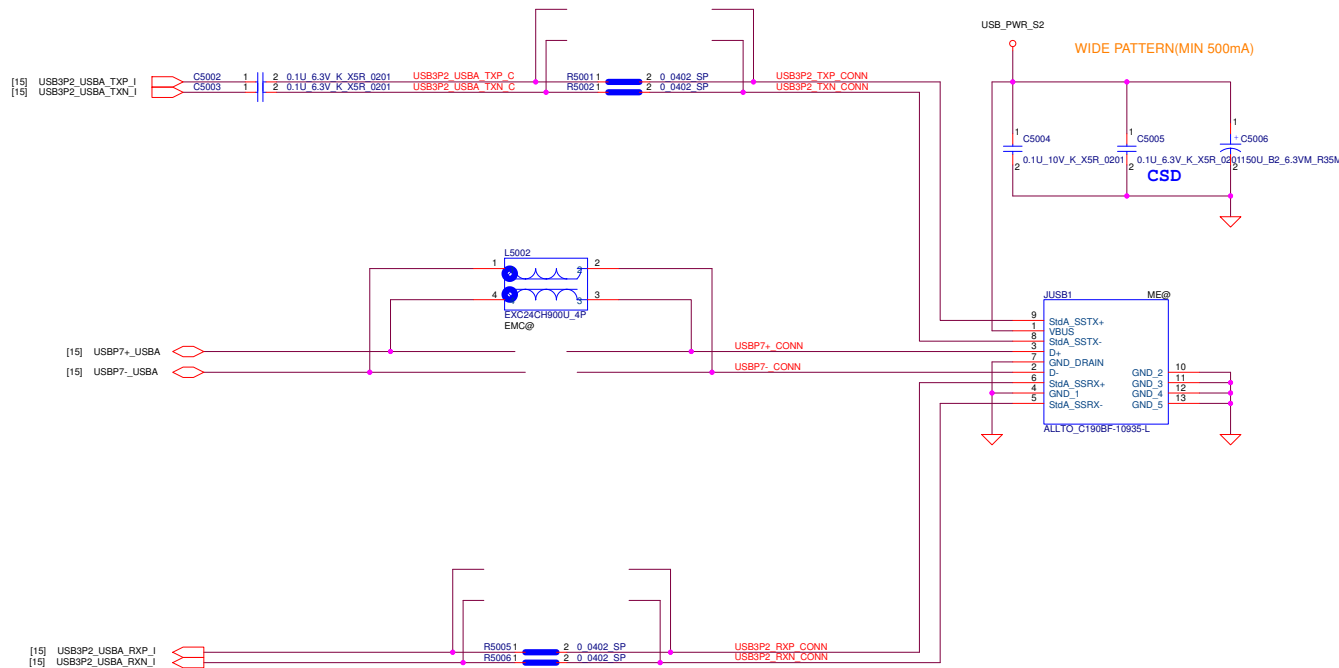
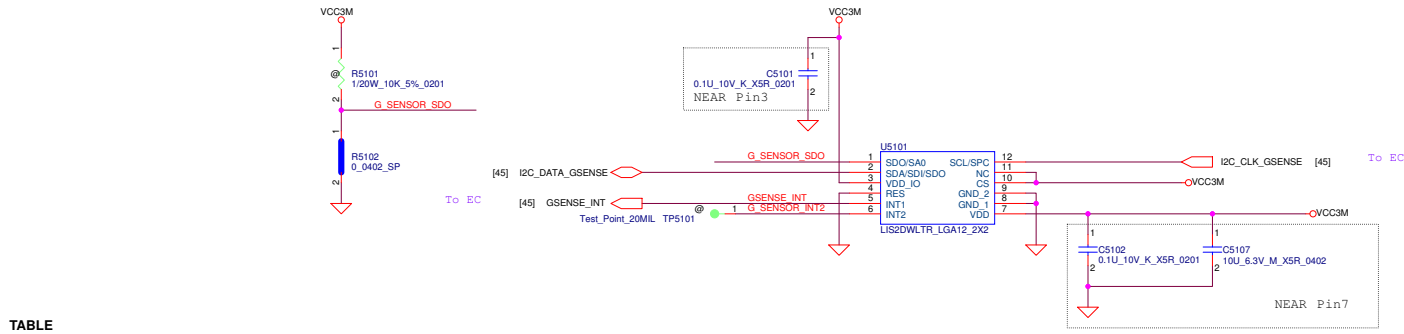


TABLE of USB3.0 Single		LCFC P/N
TI	TPS2069CDGNR	SA00005TE00

Need double confirm 2nd source



G-SENSOR

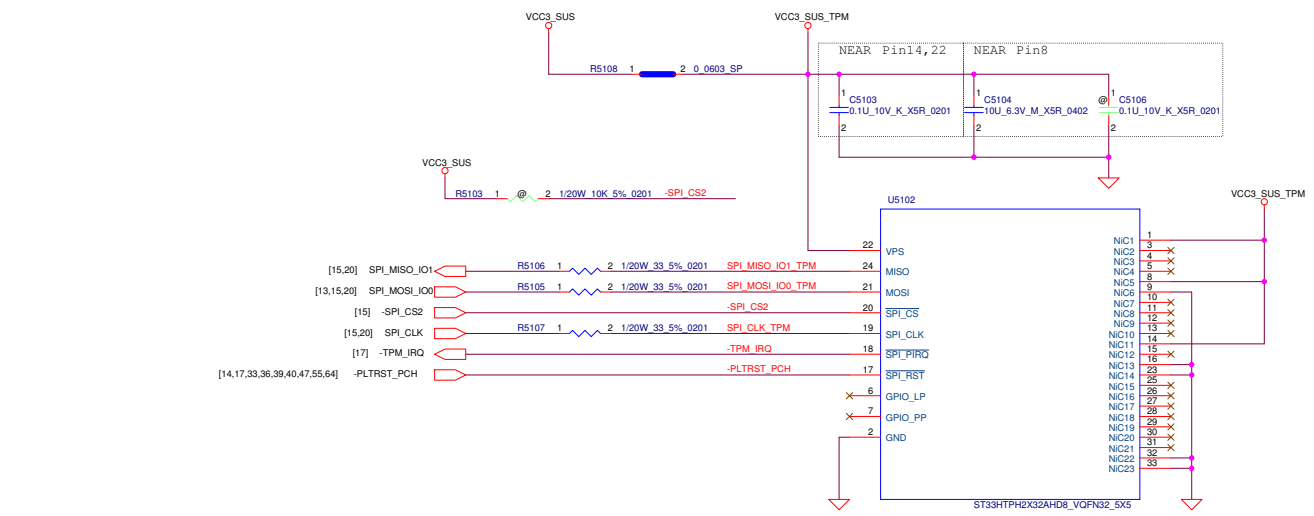


TABLE

Vendor	ADDR_SEL	Address
Kionix	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
ST	H L	32h (W) & 33h (R) 30h (W) & 31h (R)

TABLE of G-Sensor (GSU1)			
Vendor	Mfr. P/N	LCFC P/N	
Kionix	KX022-1020	SA000081E00	
ST	LIS2DWLTR	SA00009AQ00	

DISCRETE TPM 2.0



- 1. To be confirm dTPM FW version.
- 2. To be confirm how to co-design with fTPM.

TABLE

Pin No	NUVOTON NPCT750LADYX SA00008KS30	ST Micro ST33HTPH2X32AHD4 SL80X01013
1	VDD	NC
2	NC	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	GPIO3	GPI
7	NC	PP
8	VDD	NIC
9	NC	NC
10	NC	NC
11	NC	NC
12	NC	NC
13	GPIO4	NC
14	NC	NC
15	NC	NC
16	GND	NC
17	RST#	SPI RST#
18	PIRQ#	SPI PIRQ#
19	SCLK	SPI CLK
20	CS#	SPI CS#
21	MOSI	MOSI
22	VDD	VPS
23	GND	NC
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	SDA/GPIO0	NC
30	SCL/GPIO1	NC
31	NC	NC
32	NC	NC

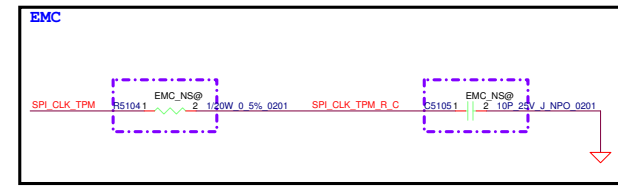
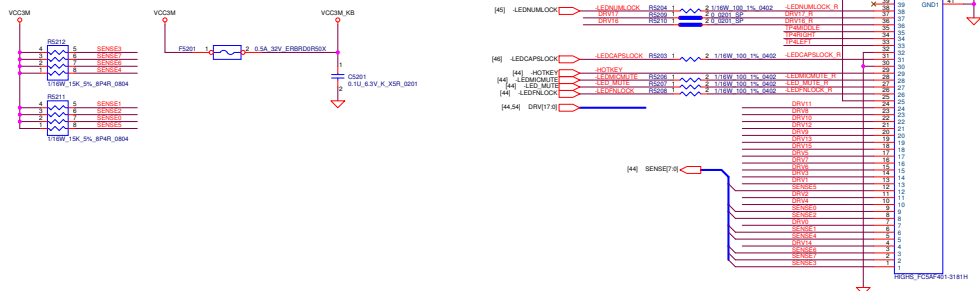
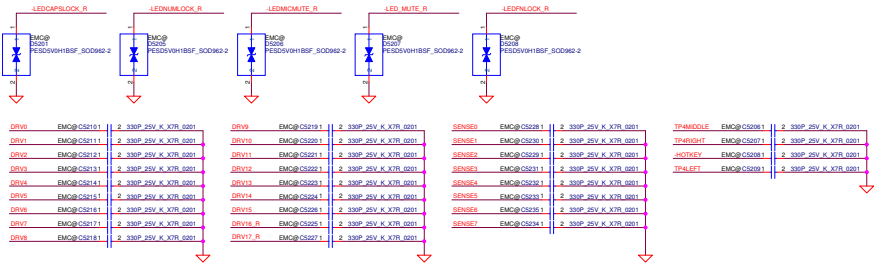


TABLE of TPM (U42)			
Vendor	P/N	LCFC P/N	Valid through
ST	ST33HTPH2X32AHD8	SA0000AB720	
NUVOTON			

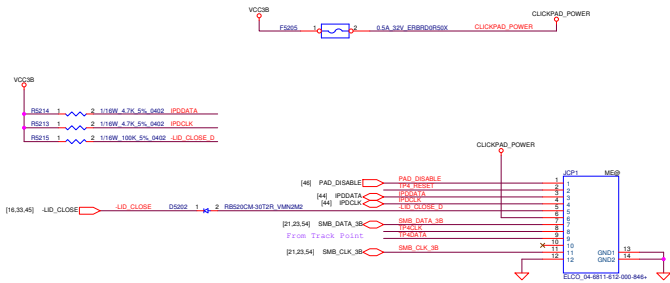
## KEYBOARD



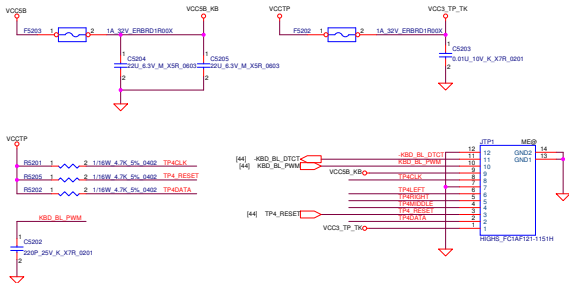
Close to JKB1



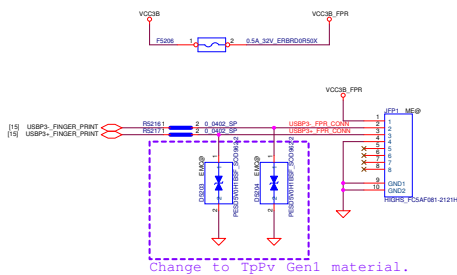
## CLICK PAD





## TRACK POINT



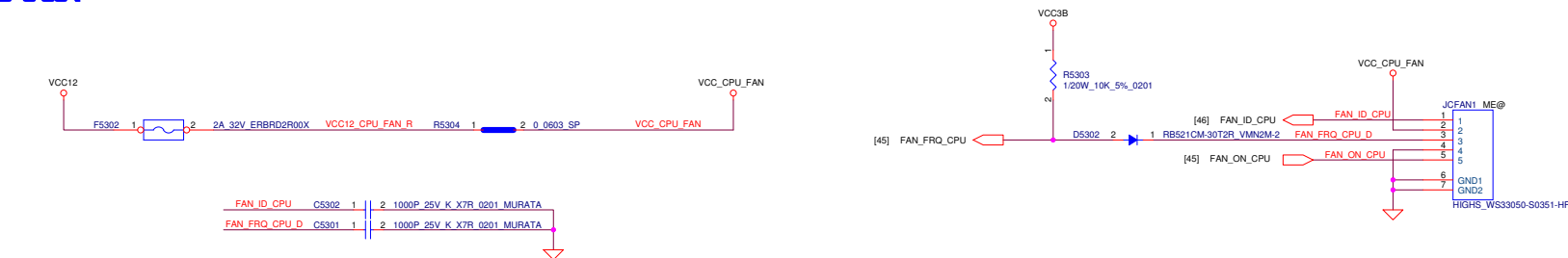
## Finger Print



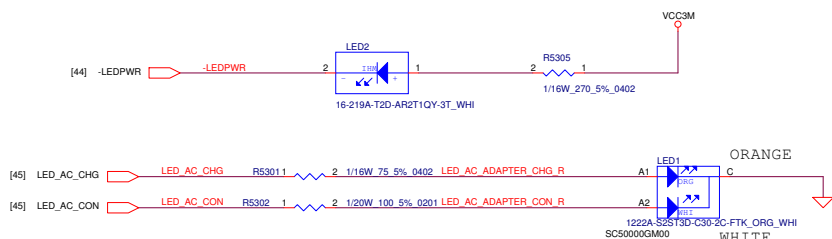
Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		KEYBOARD/TRACK POINT			
2019/12/26		yyyy/mm/dd					
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Date		Monday, May 13, 2025		Sheet		52 of 135	



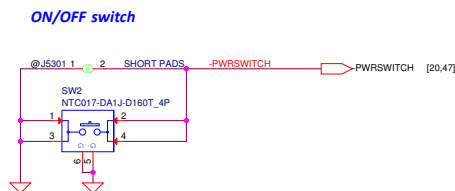
CPU FAN



AC-IN LED



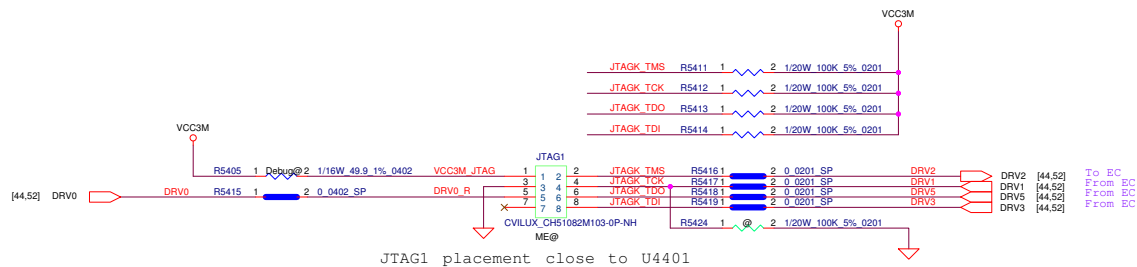
Power Switch



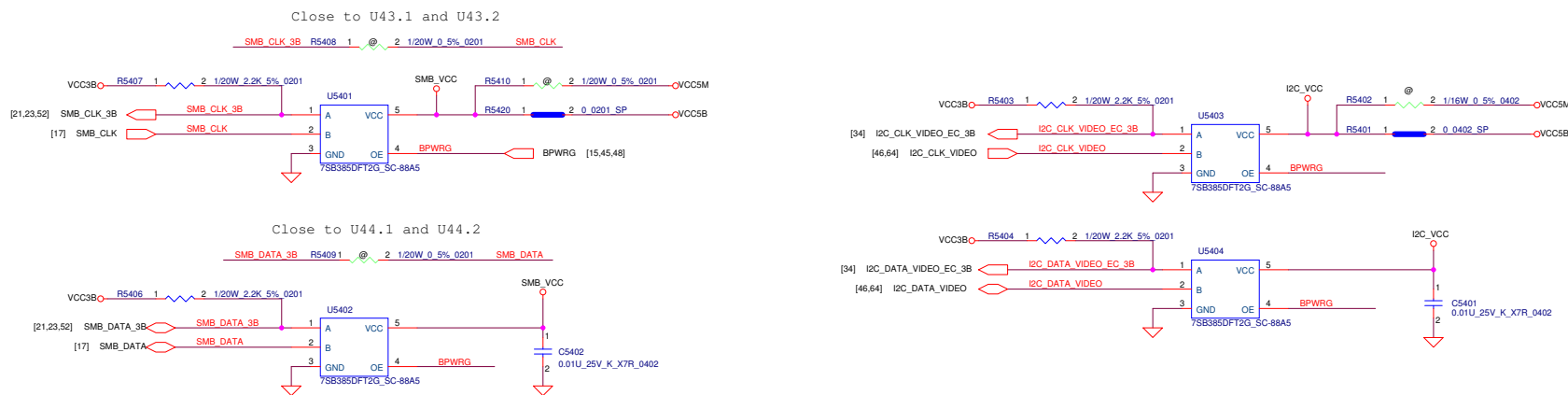
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IO/B CONN

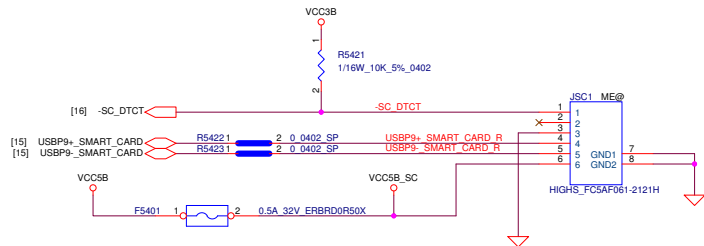
# EC DEBUG PORT



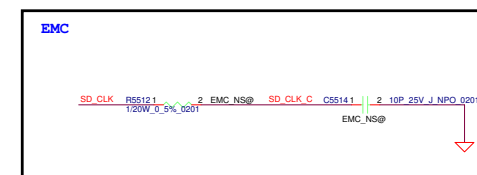
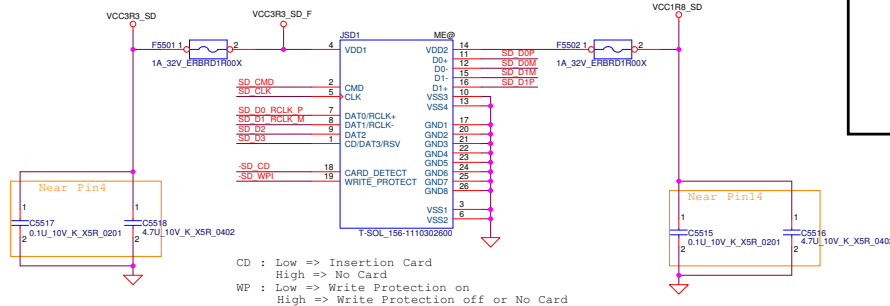
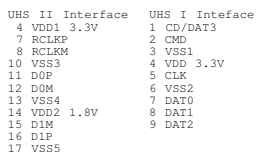
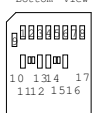
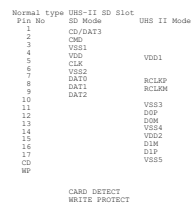
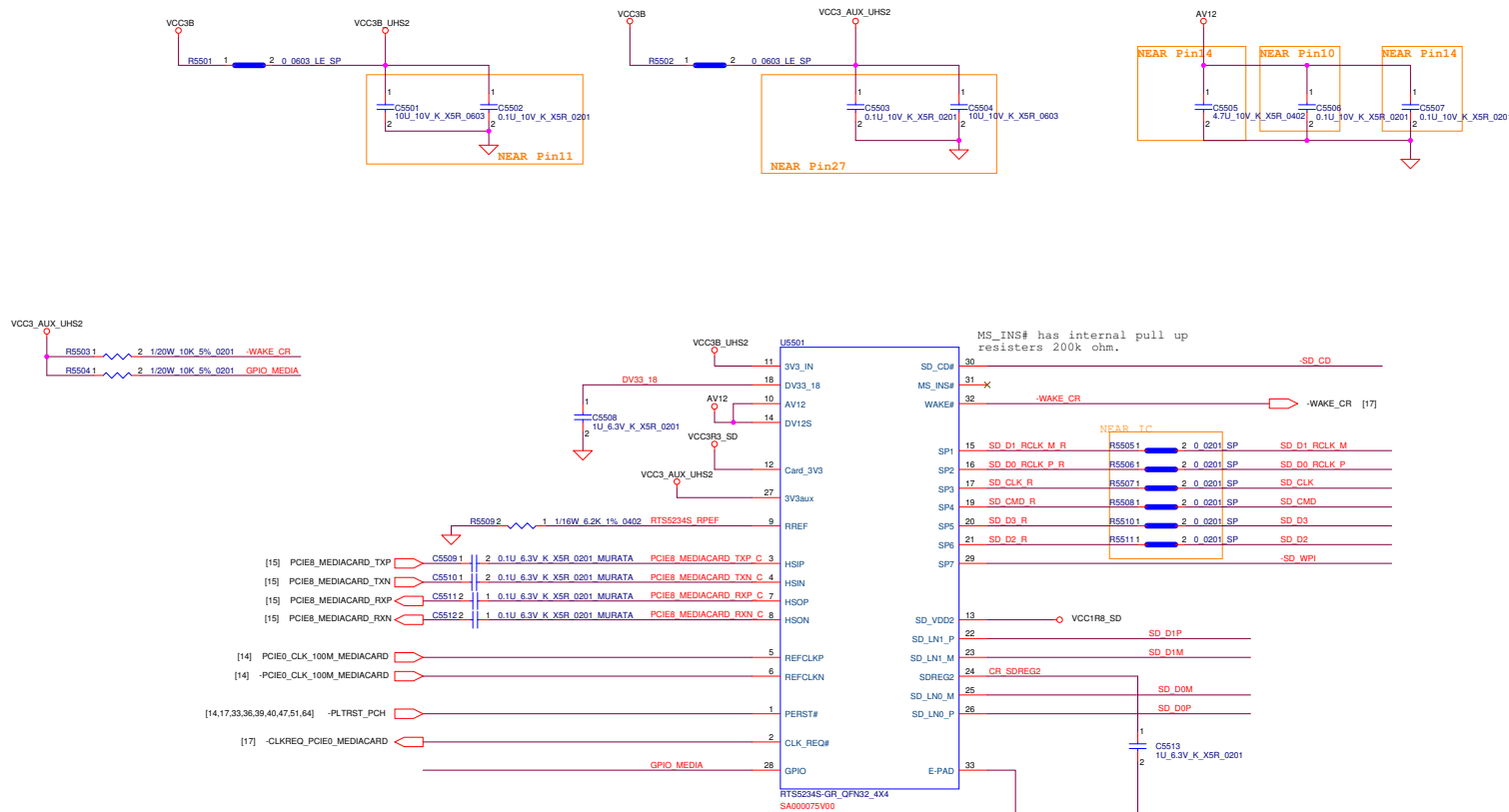
# SMBUS SWITCH




# SMART CARD




## Card Reader



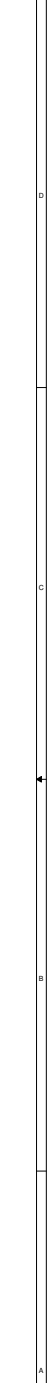
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Date: Monday, May 10, 2021					Sheet 56 of 133	

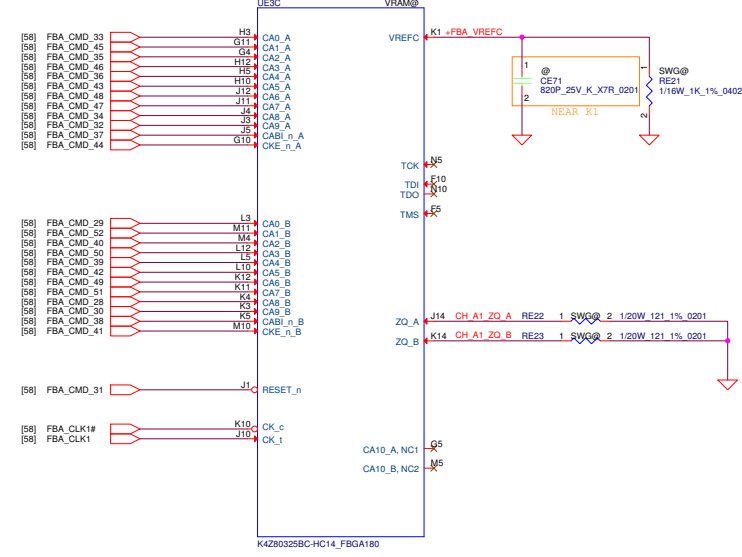
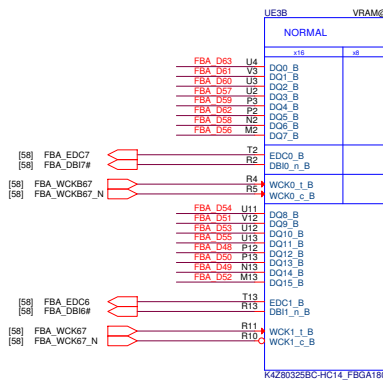
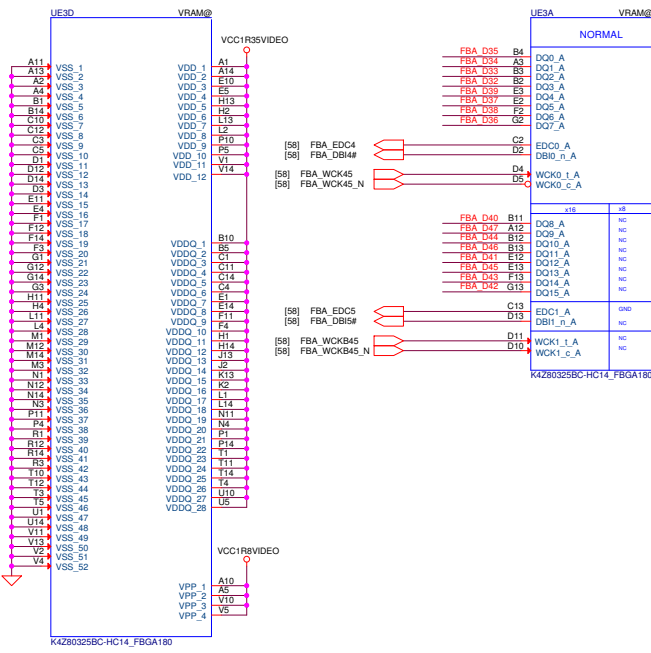
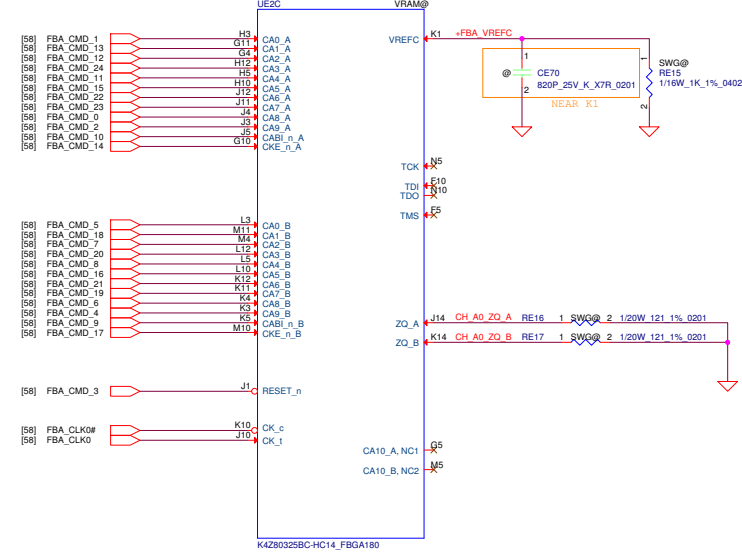
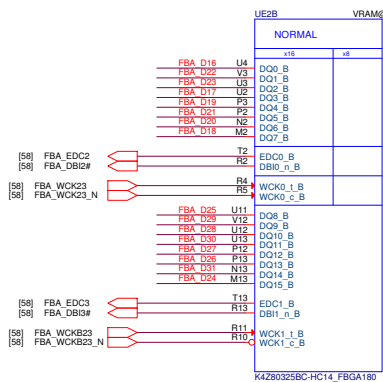
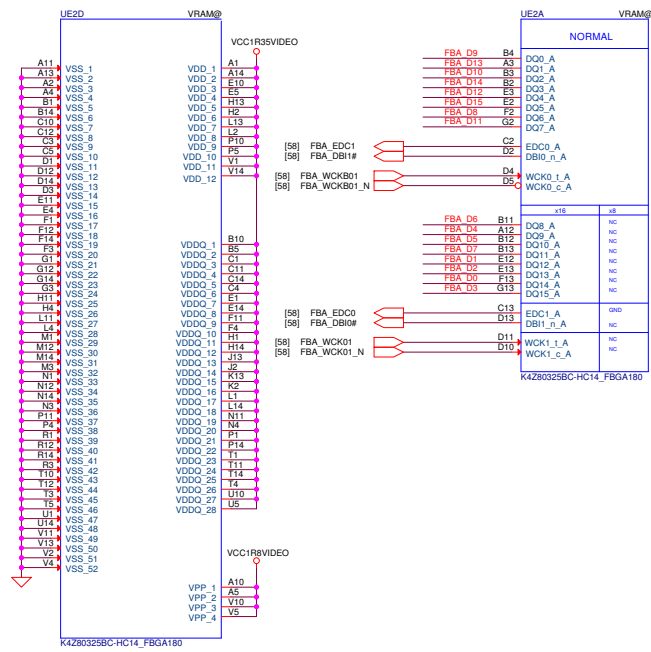
**Raptor & Blackbird Gen2**



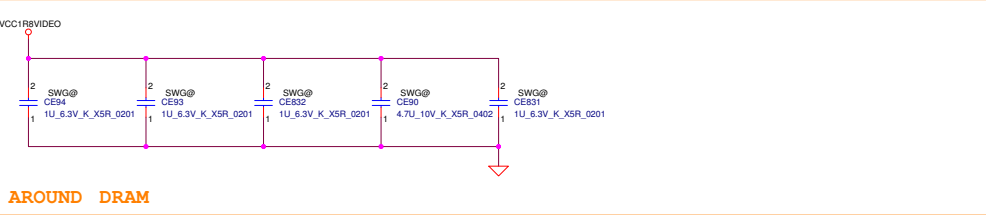
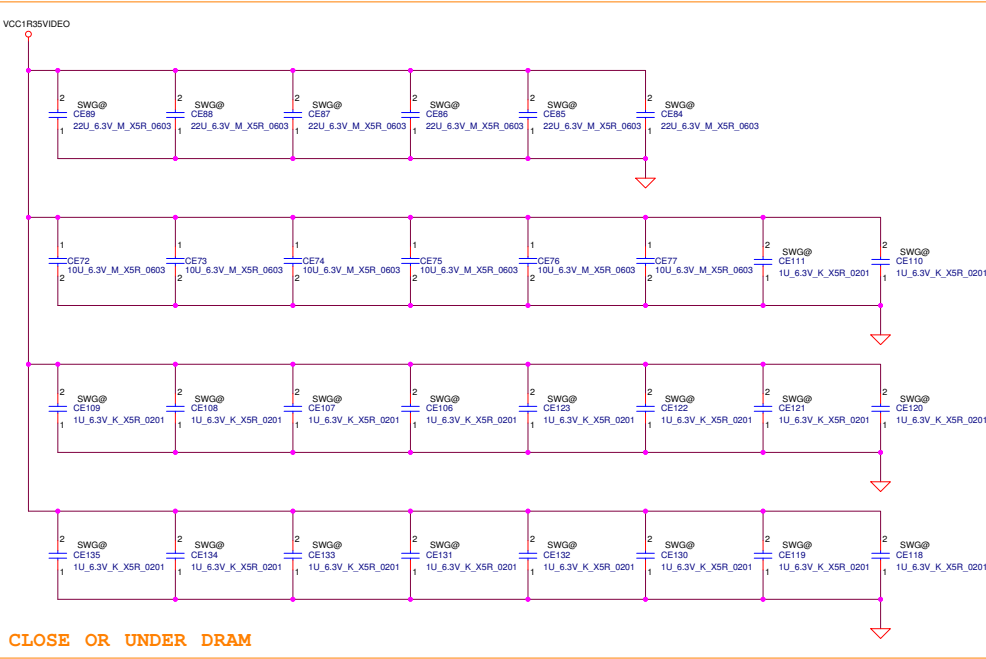


Rev 0.3	
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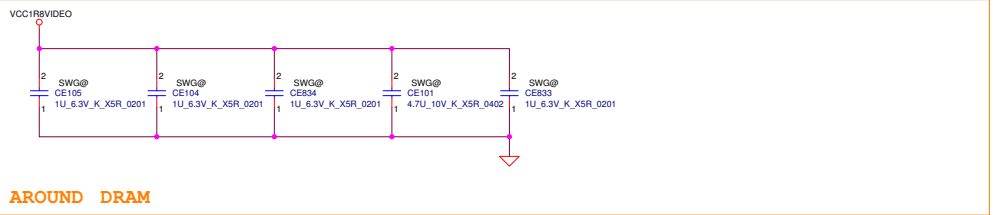
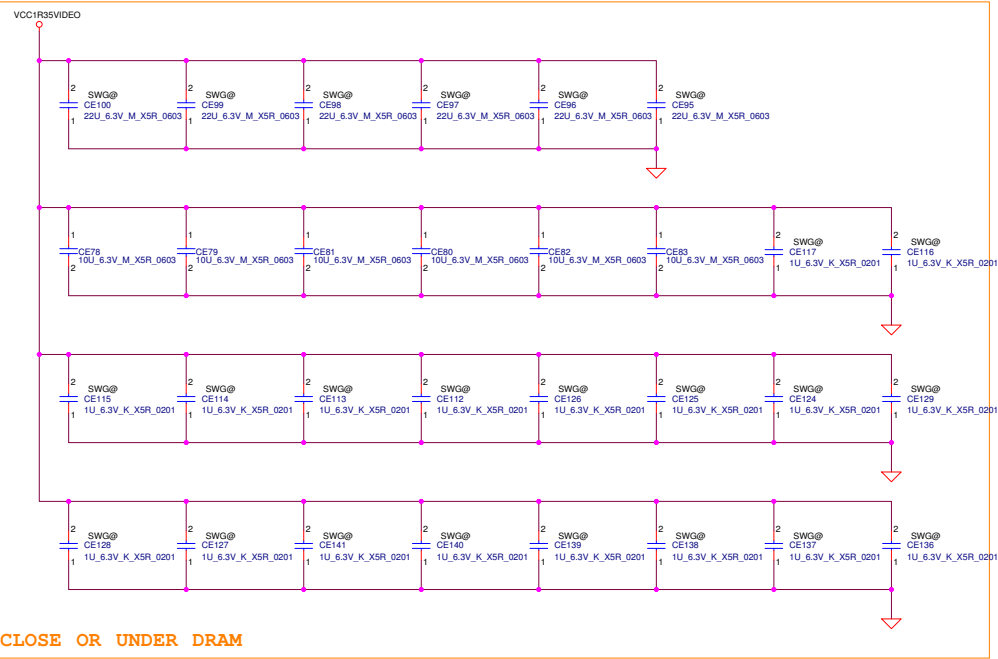
[58] FBA\_D[0..63]



UE2

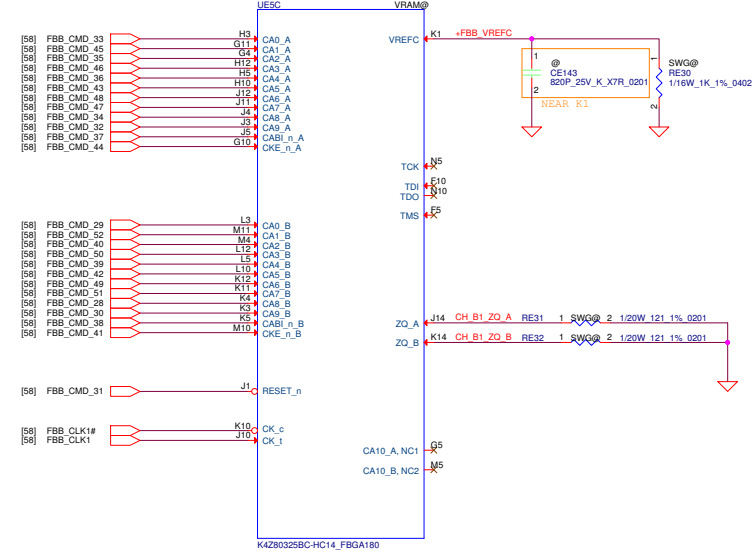
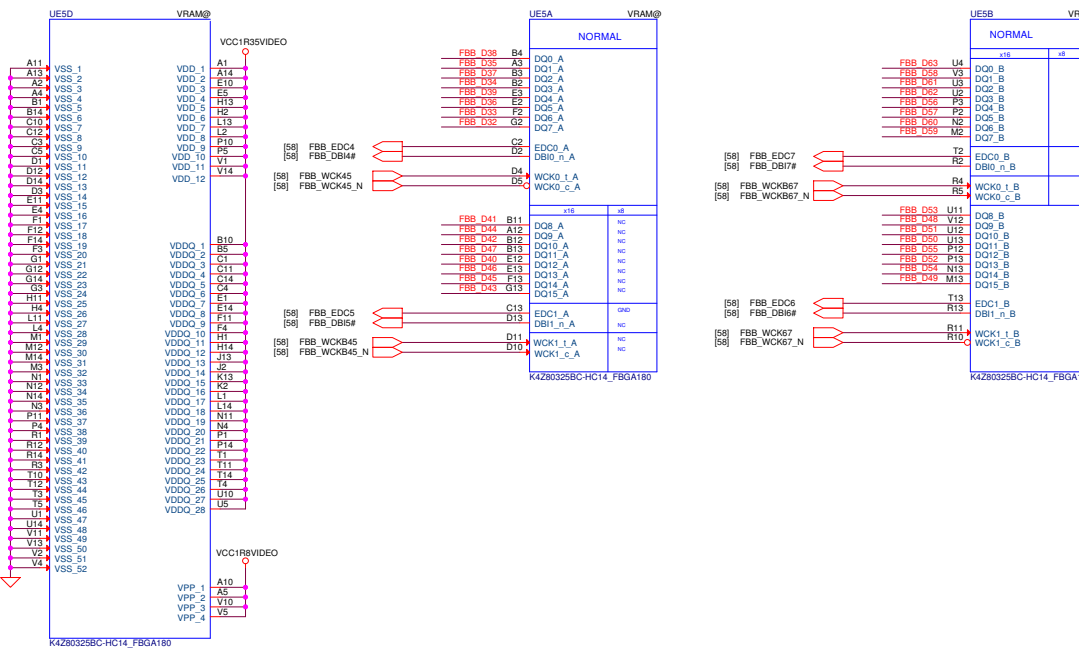
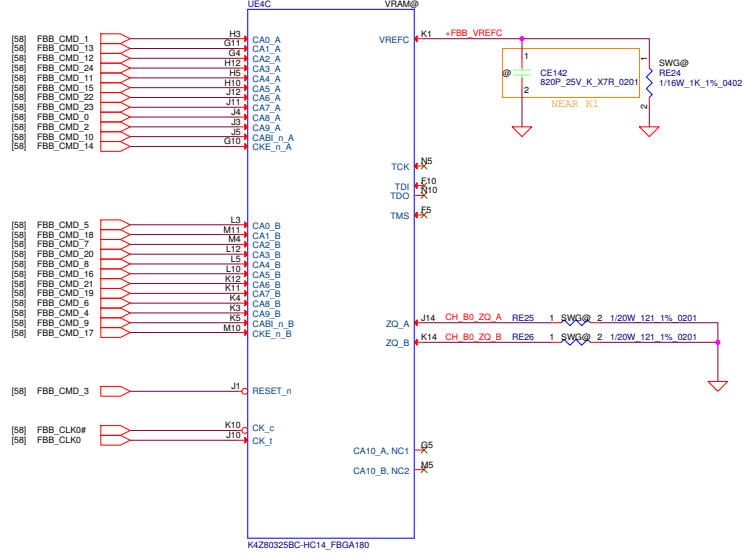
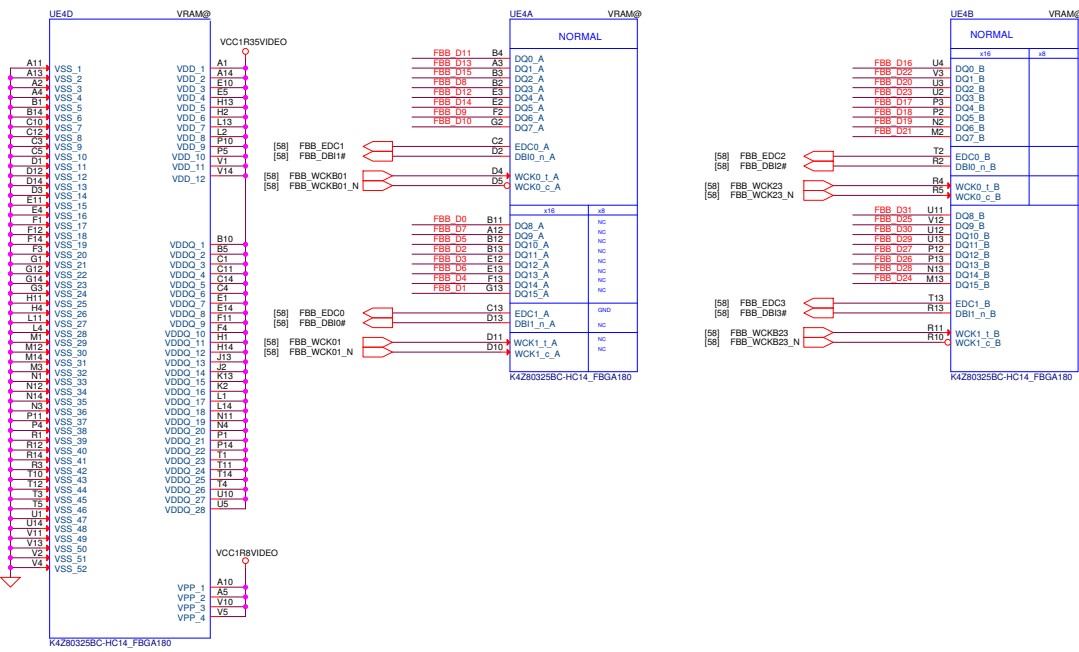


UE3

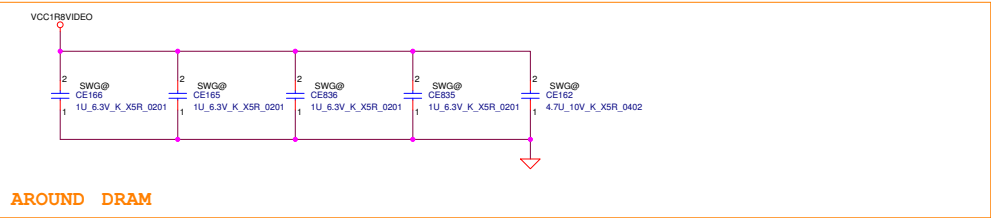
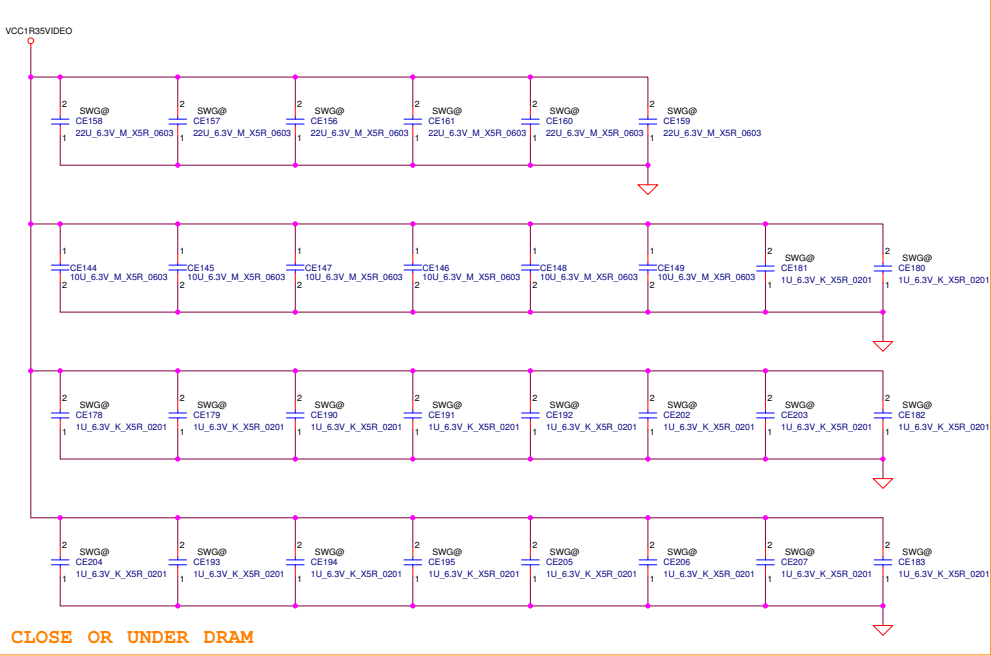




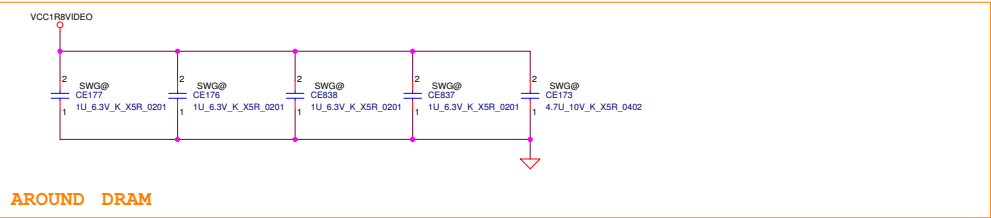
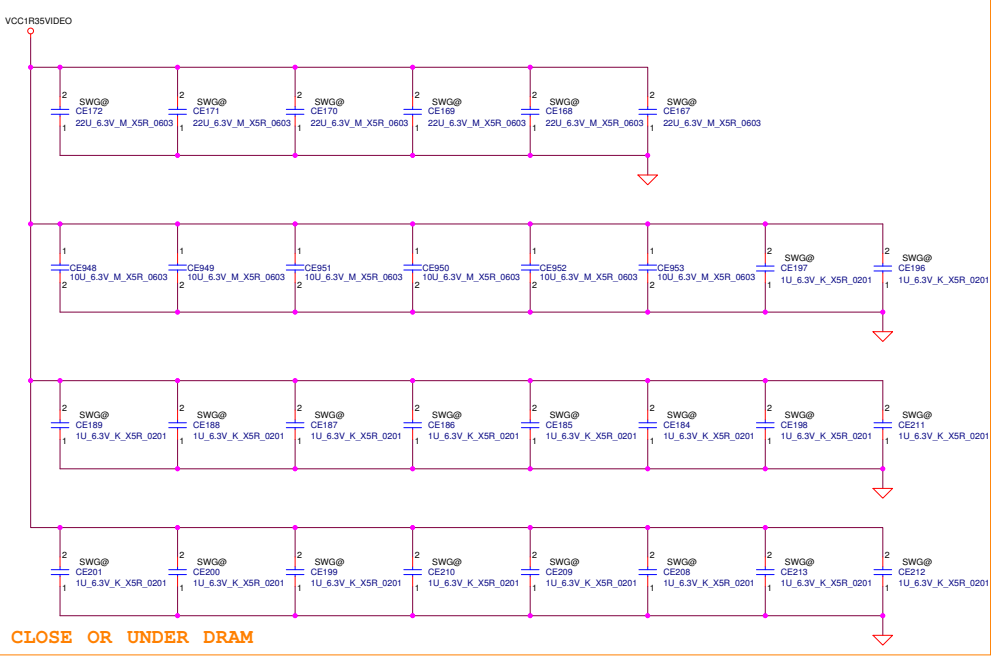
[58] FBB\_D[0..63]



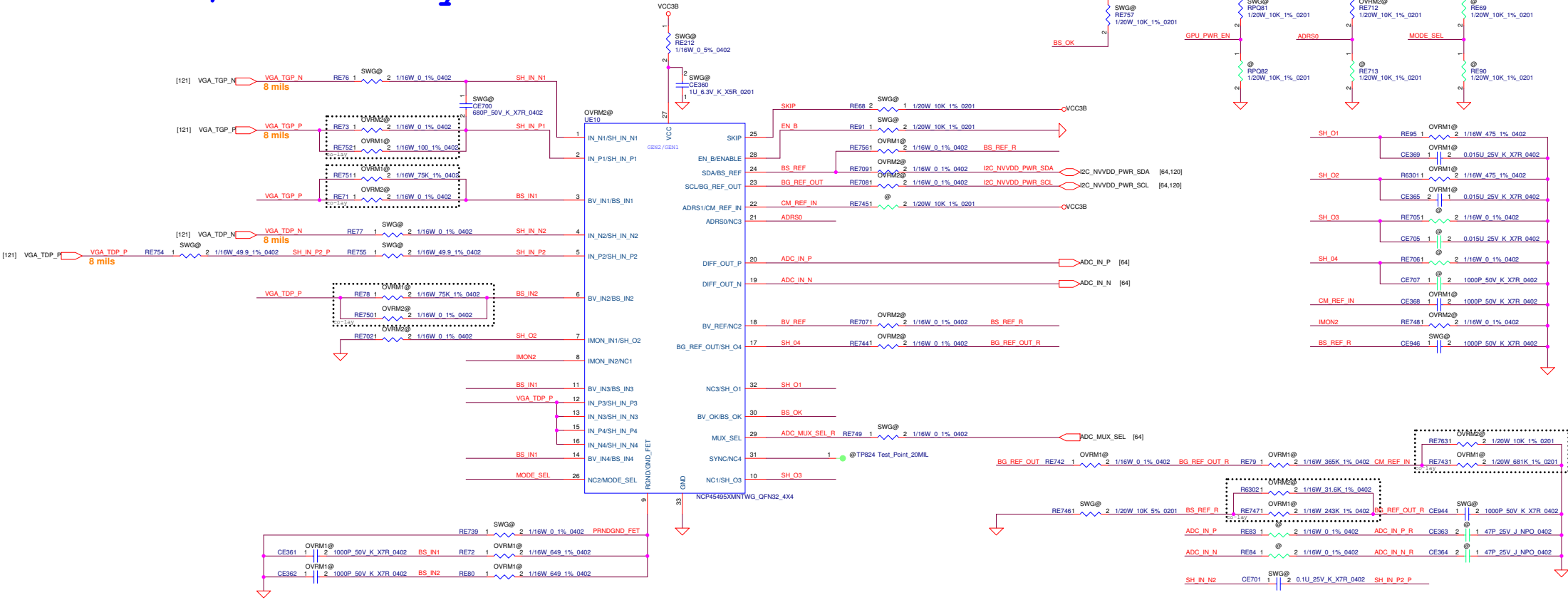
UE4



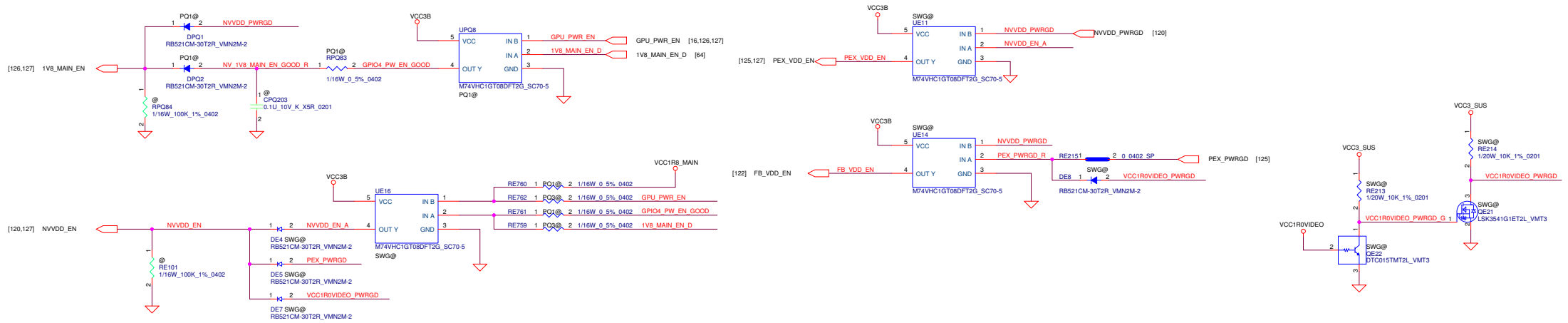
UE5



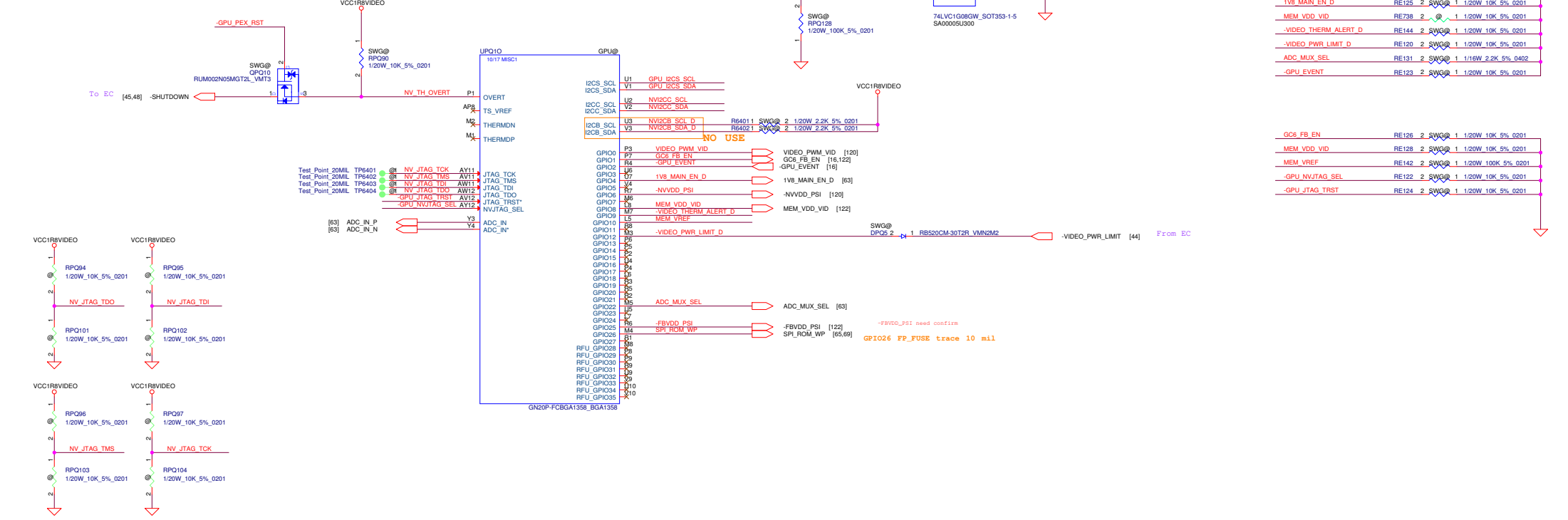
OVR-M GEN1/GEN2 co-lay



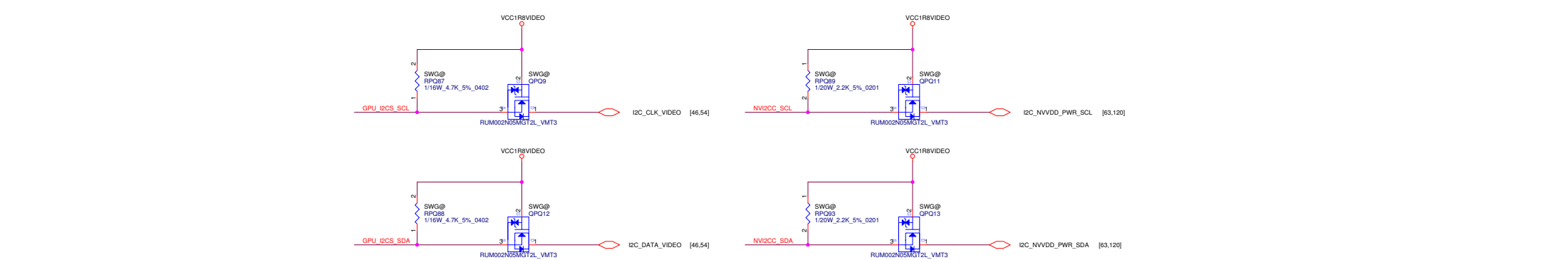
GPU power sequence

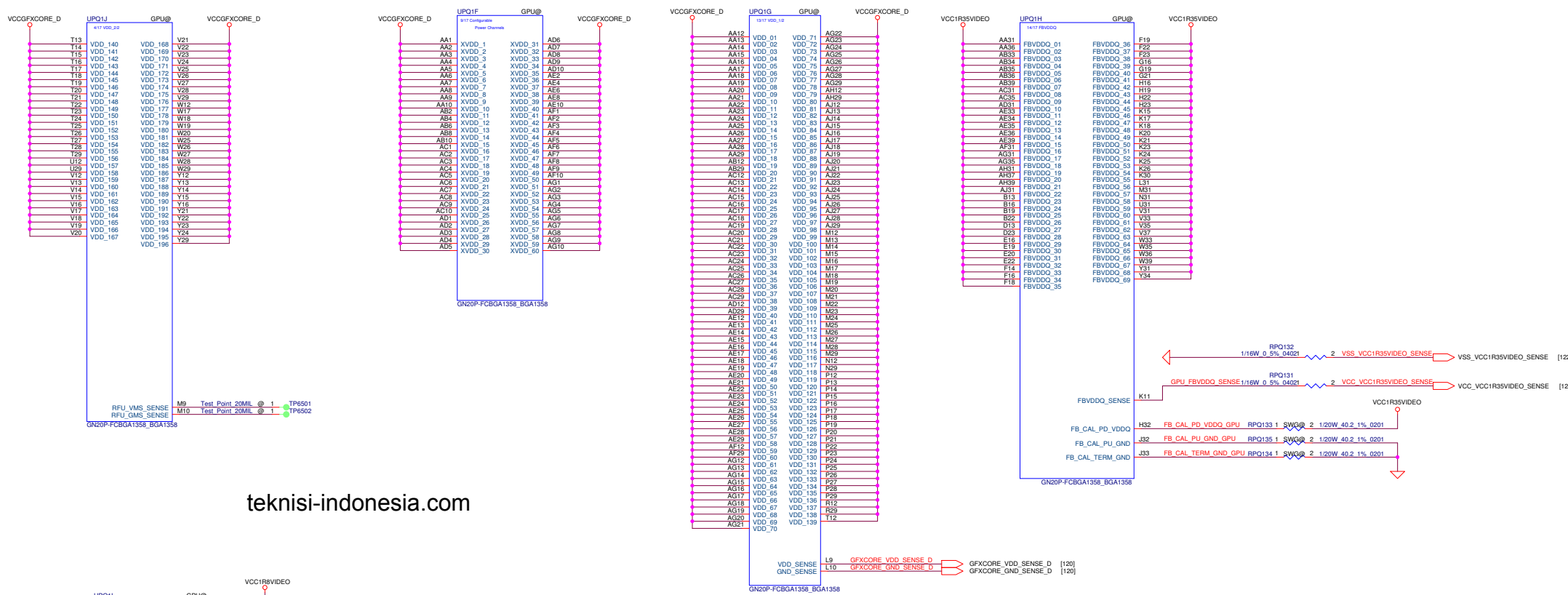


GPU

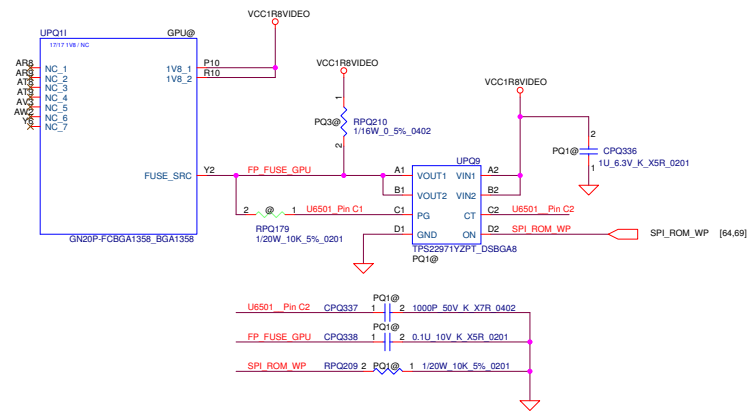


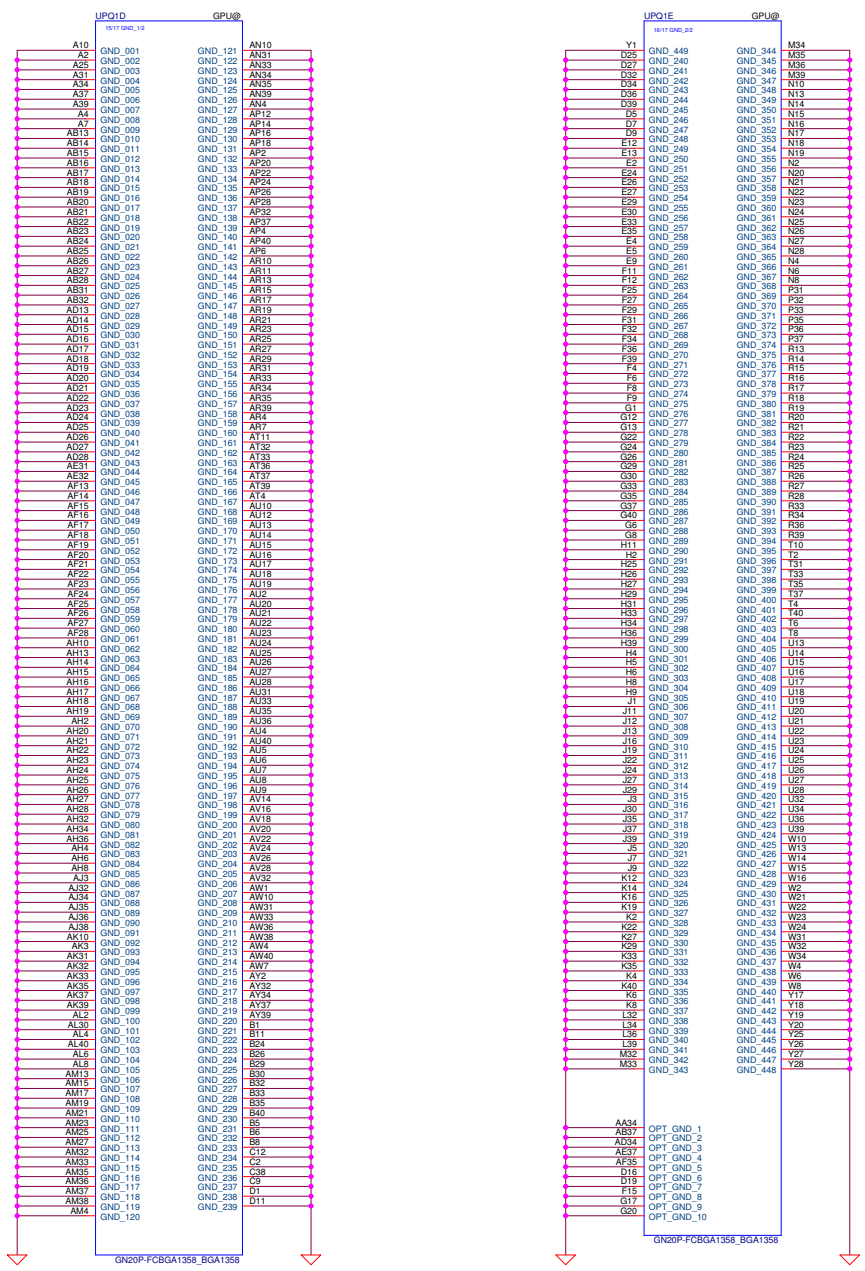
I2C level shift



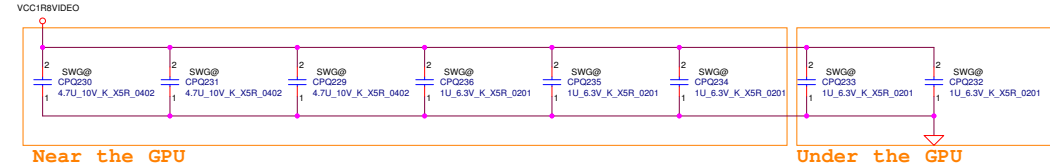
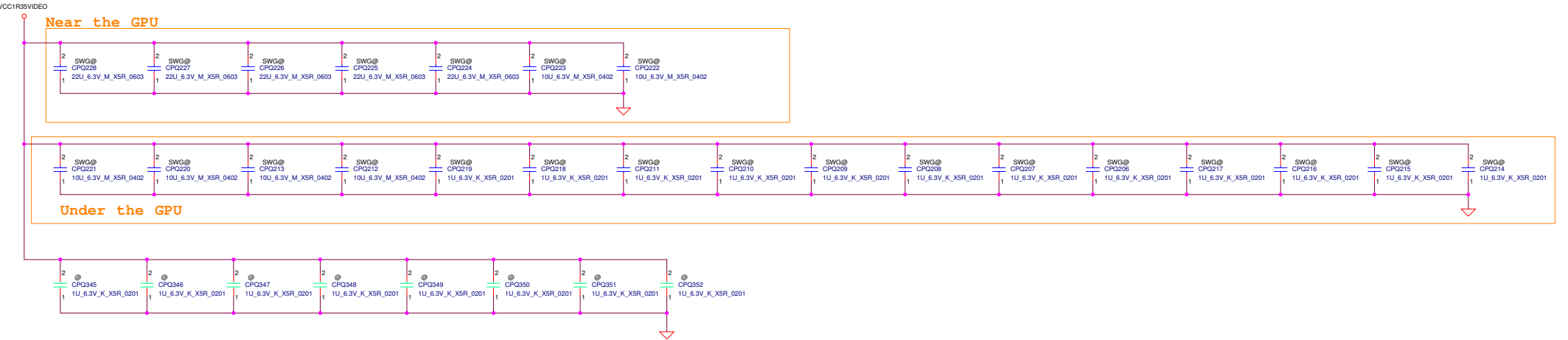
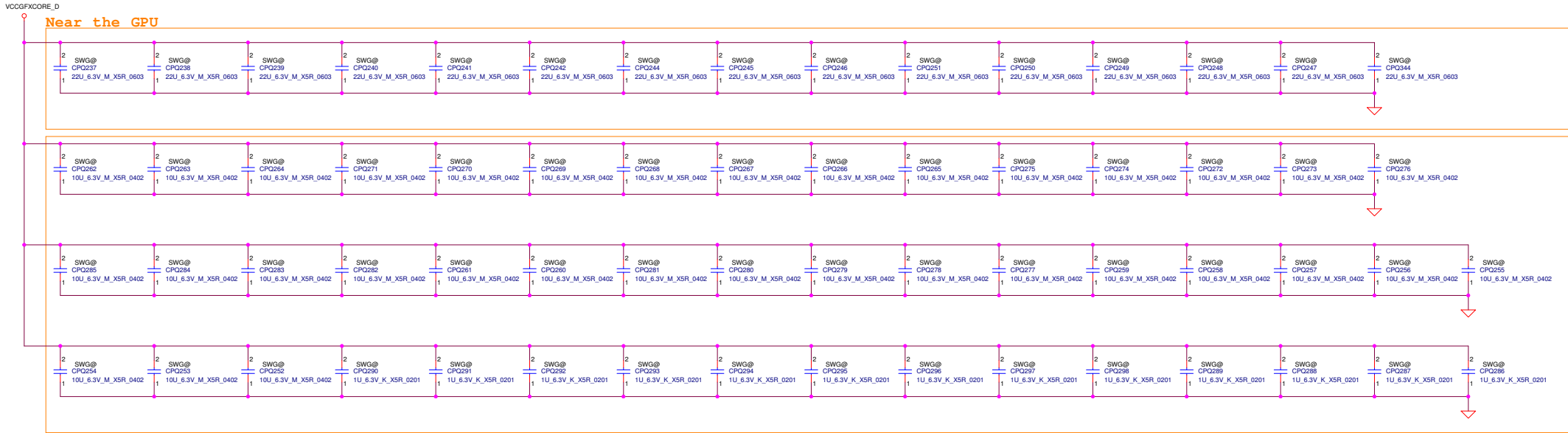


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GPU



**GPU**

**DP/IP3**

**Type-C**

**HDMI**

**DP/IP2**

**eDP**

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Title: QN20P: IFP A/B/C/D/E

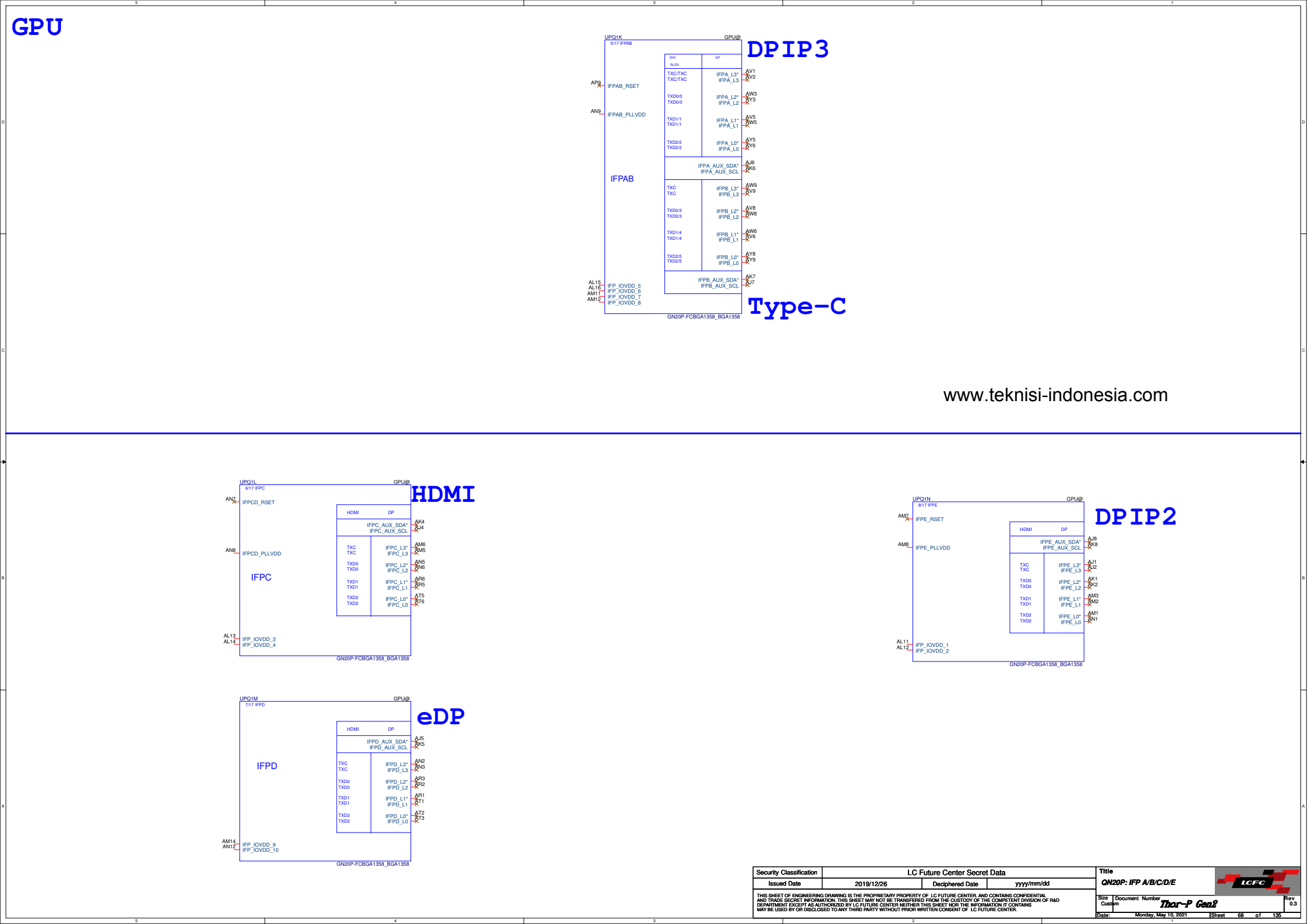
Size: 64x44mm

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

Sheet: 66 of 136

Rev: 0.3



**GPU**

**DP/IP3**

**Type-C**

**HDMI**

**DP/IP2**

**eDP**

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Issued Date: 2019/12/26

Deciphered Date: yyyy/mm/dd

Title: QN20P: IFP A/B/C/D/E

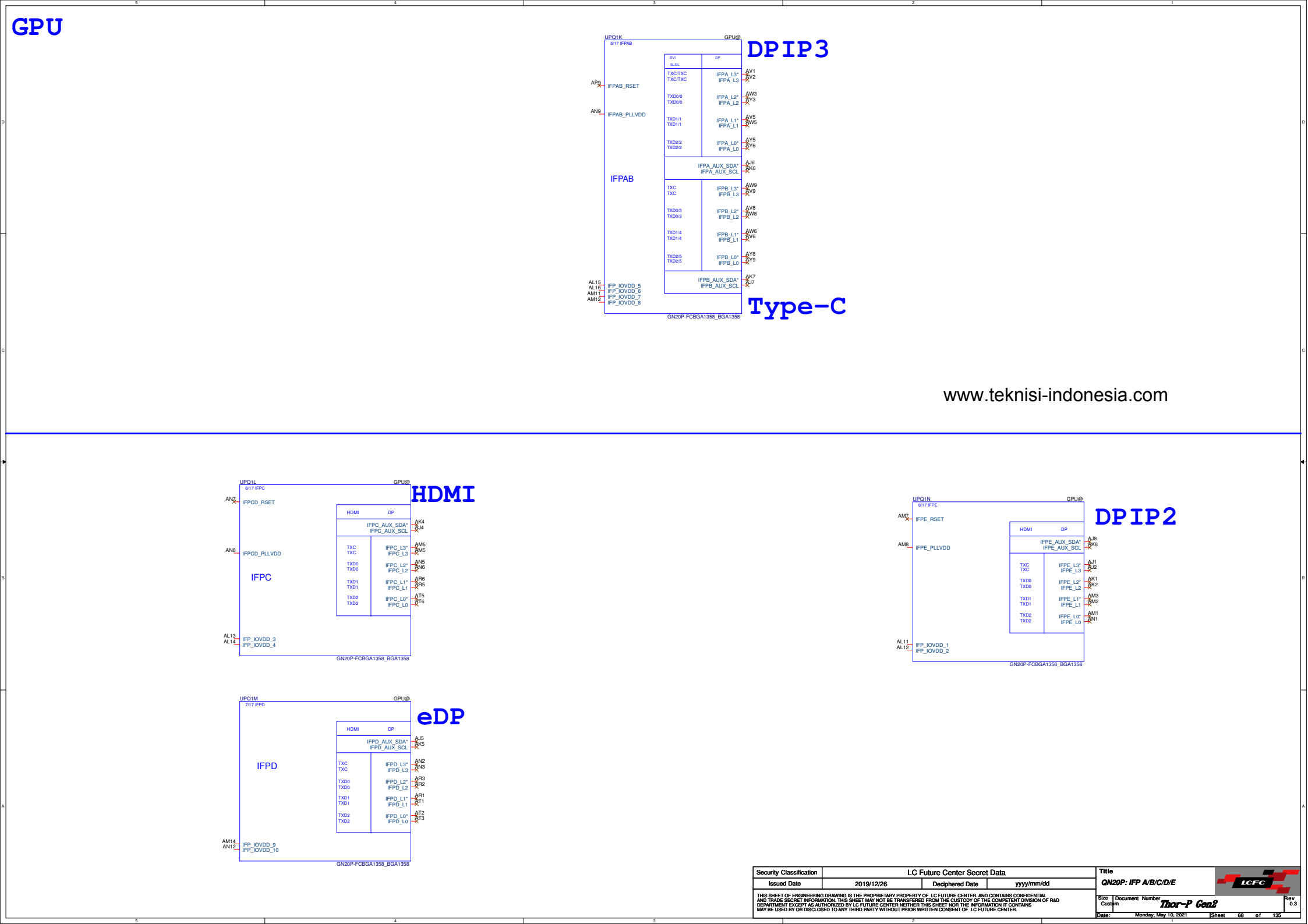
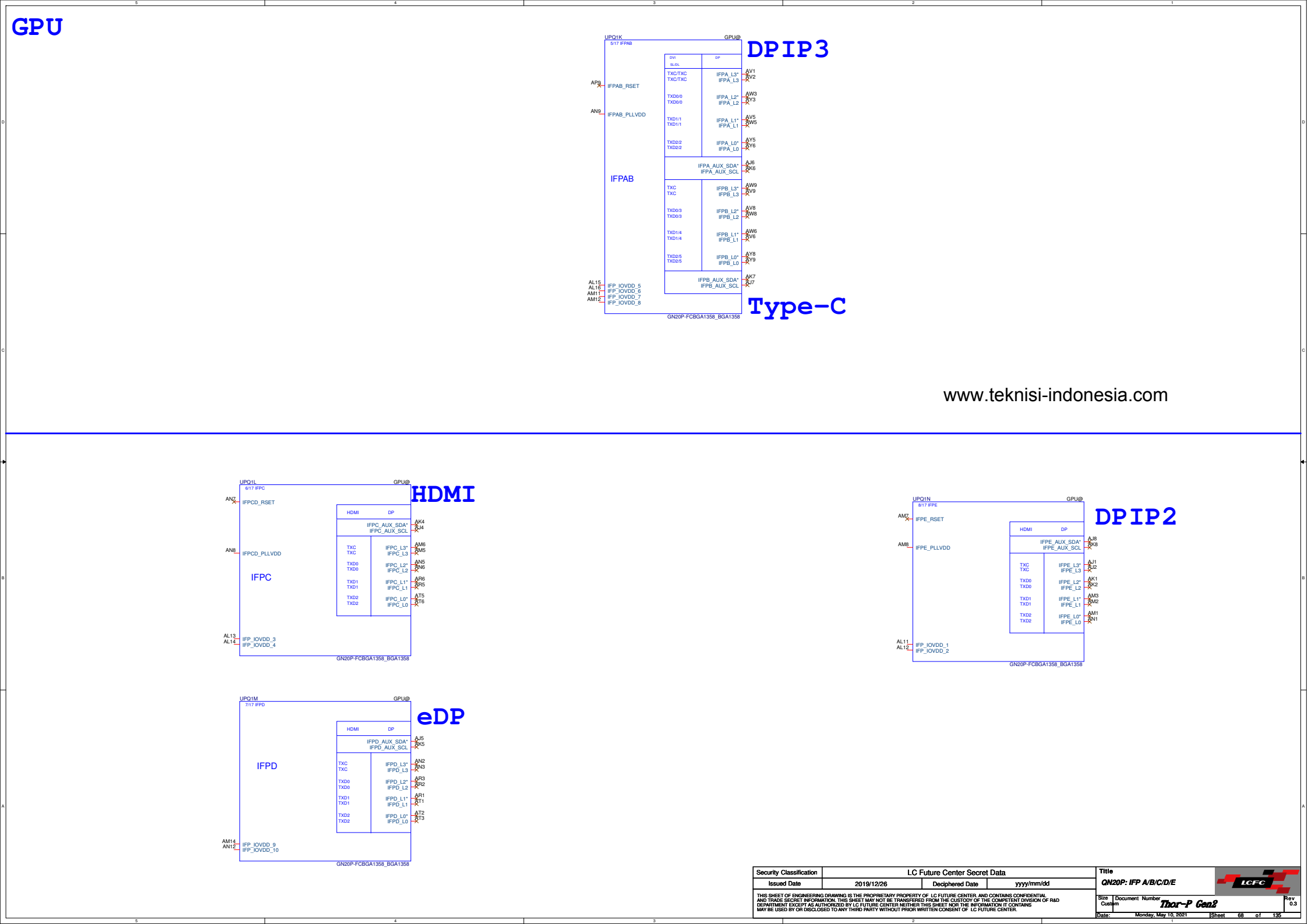
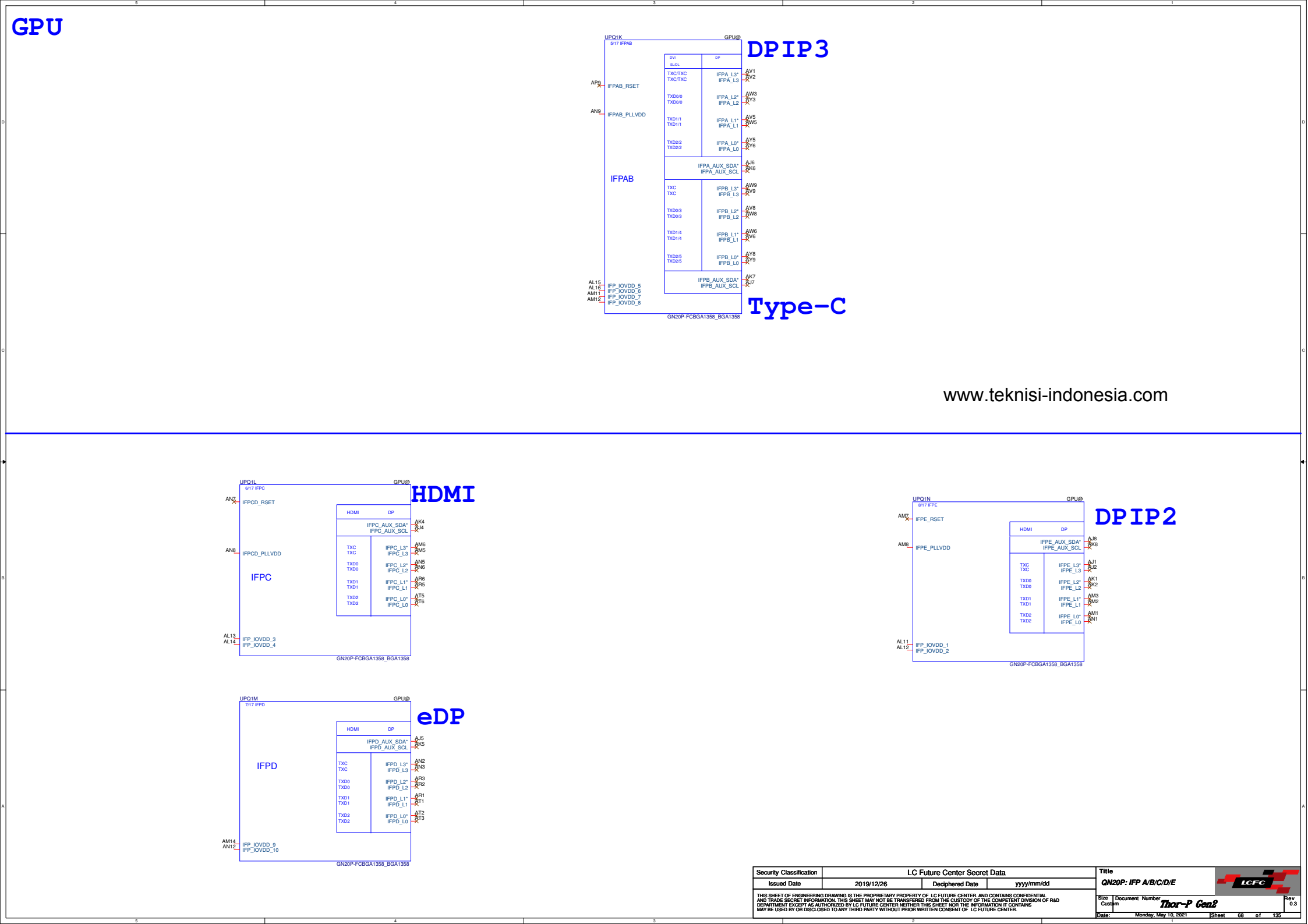
Size: 64x44mm

Document Number: Thor-P Gen2

Date: Monday, May 10, 2021

Sheet: 66 of 136

Rev: 0.3



**GPU**

**DP/IP3**

**Type-C**

**HDMI**

**DP/IP2**

**eDP**

**GN20P-FCBGA1358\_BGA1358**

**Security Classification**

**LC Future Center Secret Data**

**Issued Date** 2019/12/26 **Deciphered Date** yyyy/mm/dd

**Title** QN20P: IFP A/B/C/D/E

**Size** 64x44mm **Document Number** Thor-P Gen2 **Rev** 0.3

**Date:** Monday, May 10, 2021 **Sheet** 66 **of** 136



GPU VRAM STRAP TABLE				STRAP 0		STRAP 1		STRAP 2	
				STRAP0_H@	STRAP0_L@	STRAP1_H@	STRAP1_L@	STRAP2_H@	STRAP2_L@
GPU	Vendor	DIE Rev	Strap	R6904	R6912	R6902	R6913	R6905	R6914
QN20-P1/P3	Samsung	C-die	0x0		V		V		V
	Micron	A-die	0x1	V			V		V
	Hynix	A-die	0x2		V	V			V

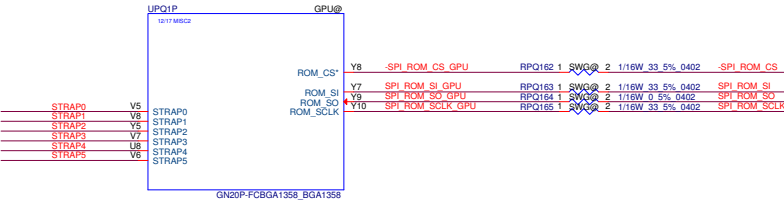
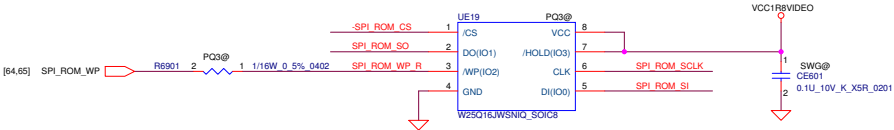


Table 9.3 RAMCFG

Strap Pins <small>see Note</small>			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
H	L	M	16 [0x0010]	
H	M	L	17 [0x0011]	
H	M	H	18 [0x0012]	
H	H	M	19 [0x0013]	
L	M	M	20 [0x0014]	
M	L	M	21 [0x0015]	
M	M	L	22 [0x0016]	
M	M	H	23 [0x0017]	
M	H	M	24 [0x0018]	
H	M	M	25 [0x0019]	
M	M	M	26 [0x001A]	

Table 9.3 RAMCFG

Strap Pins <small>see Note</small>			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 [0x0000]	
L	L	H	1 [0x0001]	
L	H	L	2 [0x0002]	
L	H	H	3 [0x0003]	
H	L	L	4 [0x0004]	
H	L	H	5 [0x0005]	
H	H	L	6 [0x0006]	
H	H	H	7 [0x0007]	
L	L	M	8 [0x0008]	
L	M	L	9 [0x0009]	
L	M	H	10 [0x000A]	
L	H	M	11 [0x000B]	
M	L	L	12 [0x000C]	
M	L	H	13 [0x000D]	
M	H	L	14 [0x000E]	
M	H	H	15 [0x000F]	



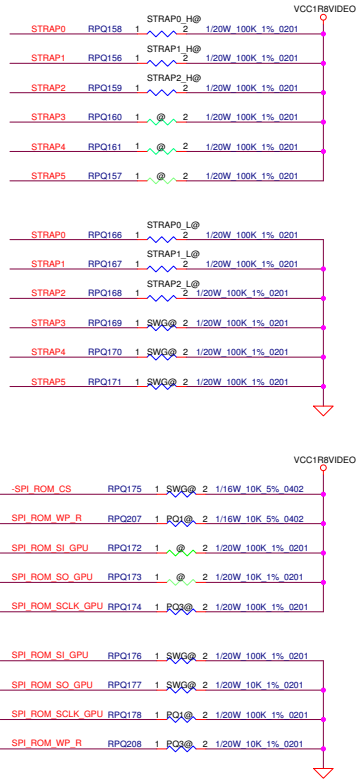
QN20-PQ1 (8Mb)	ROM	SA000080E00	W25Q80EWSNIG_SO8
QN20-PQ3 (16Mb)	ROM	SA0000A0U50	W25Q16JWSNIQ_SOIC8

Table 9.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE


Strap Pins <small>see Note</small>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	L	M				
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
H	M	M				
M	M	M				

Table 9.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

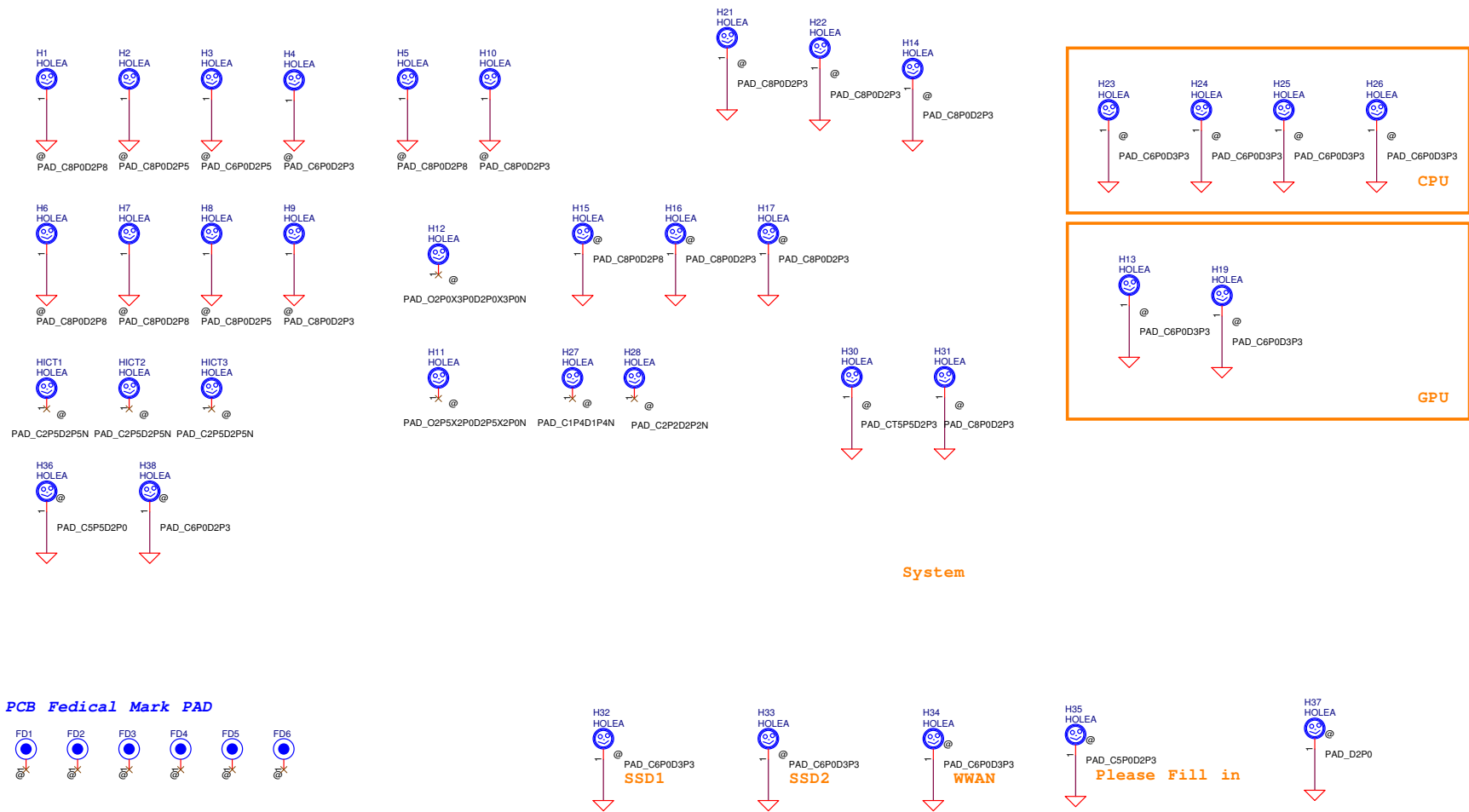
Strap Pins <small>see Note</small>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	0	0	0	0
L	M	L	1	0	0	1
L	M	H	0	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1



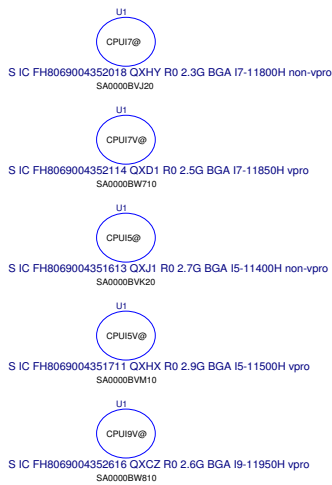
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						<small>Custm</small>	<i>Thor-P Gen2</i>	0.3
						<small>Date:</small>	Monday, May 16, 2021	<small>Sheet</small> 70 <small>of</small> 135

# Thor-P Gen2 Screw Hole & FDI



CPU



PCB



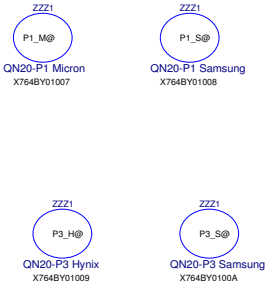
LAN



PCH

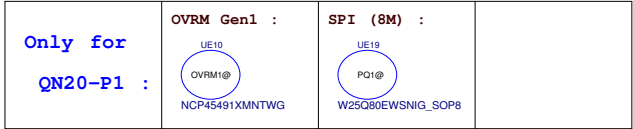
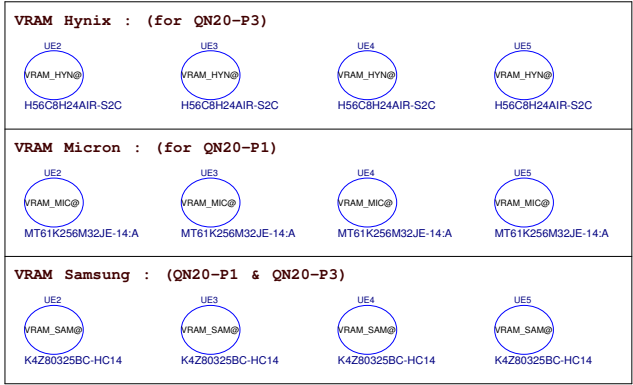
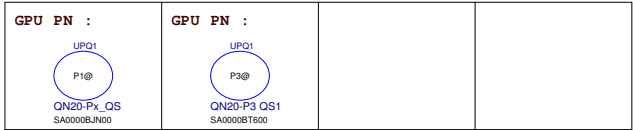


X76



GPU


the phase has ES sample only SA0000B3H10




GPU :	QN20-P1		QN20-P3	
VRAM :	Samsung	Micron	Samsung	Hynix
X76 PN :				
VRAM_SAM@	V	X	V	X
VRAM_MIC@	X	V	X	X
VRAM_HYN@	X	X	X	V
STRAP0_H@	X	V	X	X
STRAP1_H@	X	X	X	V
STRAP2_H@	X	X	X	X
STRAP0_L@	V	X	V	V
STRAP1_L@	V	V	V	X
STRAP2_L@	V	V	V	V

GPU :	QN20-P1	QN20-P3
PQ1@	V	X
PQ3@	X	V
OVRM1@	V	X
OVRM2@	X	V
SWG@	V	V
VRAM@	X	X
GPU@	X	X


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Date: Monday, May 10, 2021				Sheet 73 of 135		


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C	<i>Thor-P Gen2</i>				0.3	
Date:		Monday, May 10, 2021		Sheet		74 of 135



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C	Thor-P Gen2				0.3	
Date:		Monday, May 10, 2021		Sheet		75 of 135


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Size C	Document Number				<i>Thor-P Gen2</i>	Rev 0.3
Date: Monday, May 10, 2021						Sheet 76 of 135




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																				C		Thor-P Gen2															0.3	
																				Date: Monday, May 10, 2021					Sheet 77 of 135													
5					4					3					2					1																		


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Date: Monday, May 10, 2021				Sheet 78 of 135		


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Date	Monday, May 16, 2021		Sheet	79	181


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Date	Monday, May 16, 2021		Page	60	61

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Date: Monday, May 10, 2021						Sheet 81 of 135

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Date: Monday, May 10, 2021				Sheet 82 of 135		

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Date: Monday, May 10, 2021				Sheet 83 of 135		

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Date: Monday, May 10, 2021				Sheet 84 of 135		




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Rev	D	Document Number	Thor-P Gen2		Rev 5.1
Date	Monday, May 16, 2021		Page	85	151


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Date			Monday, May 16, 2021
Page			68 of 151

  
**Thor-P Gen2**


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C	Thor-P Gen2				0.3	
Date: Monday, May 10, 2021						Sheet 87 of 135


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C	Thor-P Gen2				0.3	
Date: Monday, May 10, 2021						Sheet 88 of 135


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Date: Monday, May 10, 2021				Sheet 89 of 135		


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Date: Monday, May 10, 2021						Sheet 90 of 135

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C	Thor-P Gen2				0.3	
Date: Monday, May 10, 2021						Sheet 91 of 135

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Date: Monday, May 10, 2021					Sheet 92 of 135	




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Date:		Monday, May 10, 2021		Sheet	93	of 136


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				Date:	Monday, May 10, 2021	Sheet 94 of 135


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Size C	Document Number				<i>Thor-P Gen2</i>	Rev 0.3
Date: Monday, May 10, 2021						Sheet 95 of 135


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C	<i>Thor-P Gen2</i>				0.3	
Date: Monday, May 10, 2021					Sheet 96 of 135	


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Size C	Document Number				<i>Thor-P Gen2</i>	Rev 0.3
Date: Monday, May 10, 2021						Sheet 97 of 135

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Date: Monday, May 10, 2021				Sheet 98 of 135		

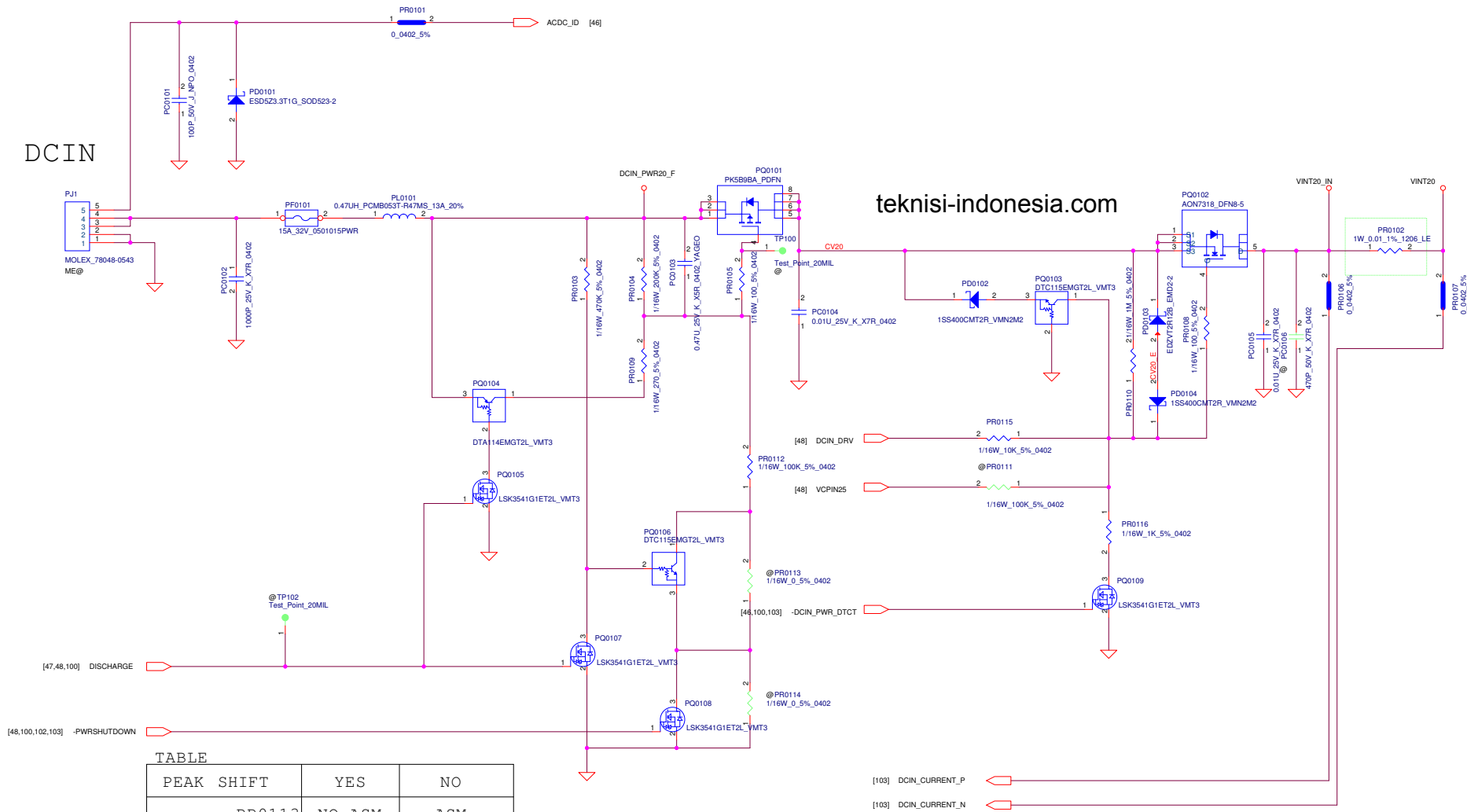
BLANK

Security Classification		LC Future Center Secret Data		Title		
Issued Date		2019/12/26	Deciphered Date	yyyy/mm/dd	BLANK	
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Size C	Document Number				<i>Thor-P Gen2</i>	Rev 0.3
Date: Monday, May 10, 2021						Sheet 99 of 135





DCIN

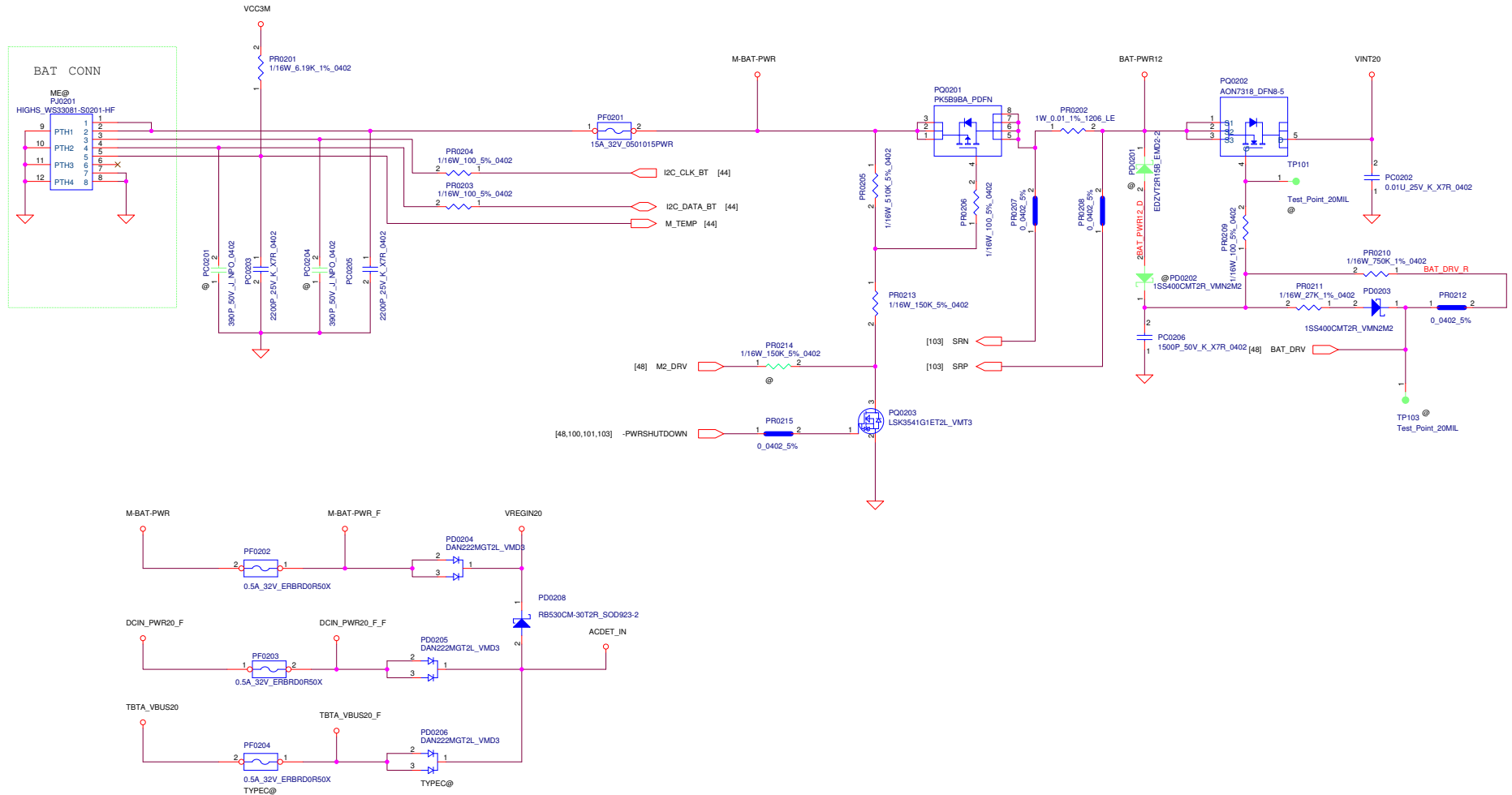


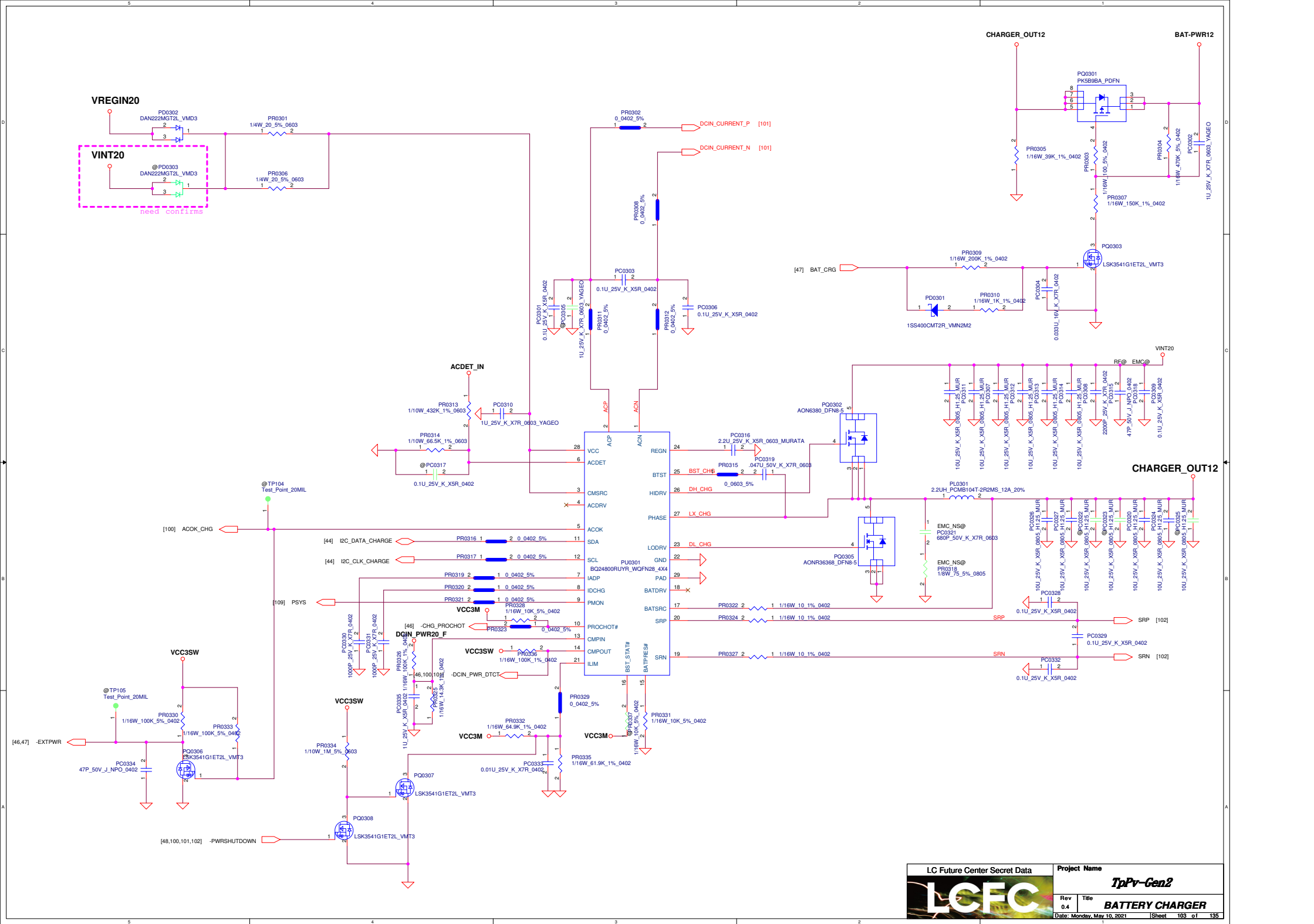
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TABLE

PEAK SHIFT	YES	NO
PR0113	NO-ASM	ASM
PR0103	ASM	NO-ASM
PQ0106	ASM	NO-ASM
PQ0107	ASM	NO-ASM

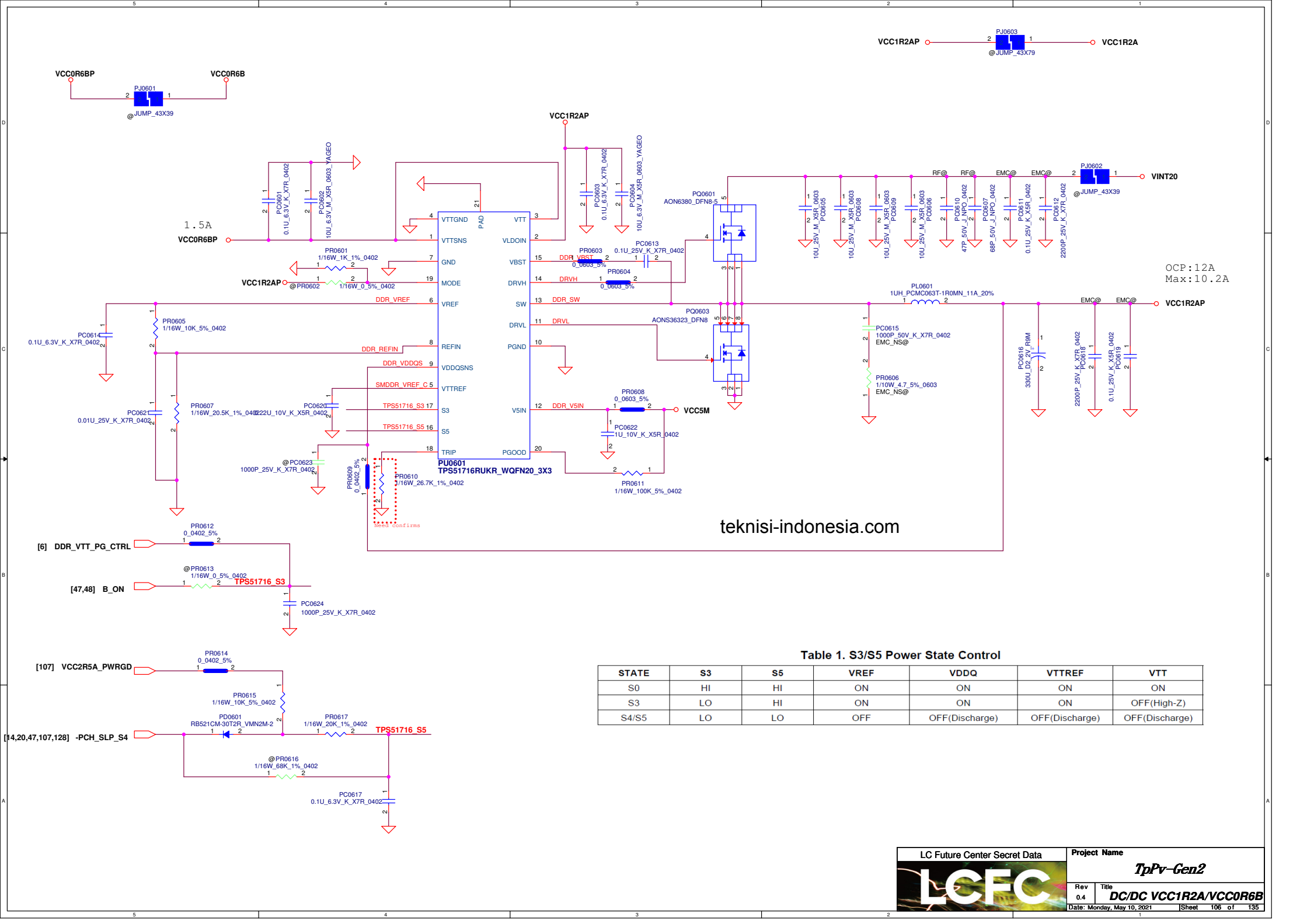
↑  
LOGIC

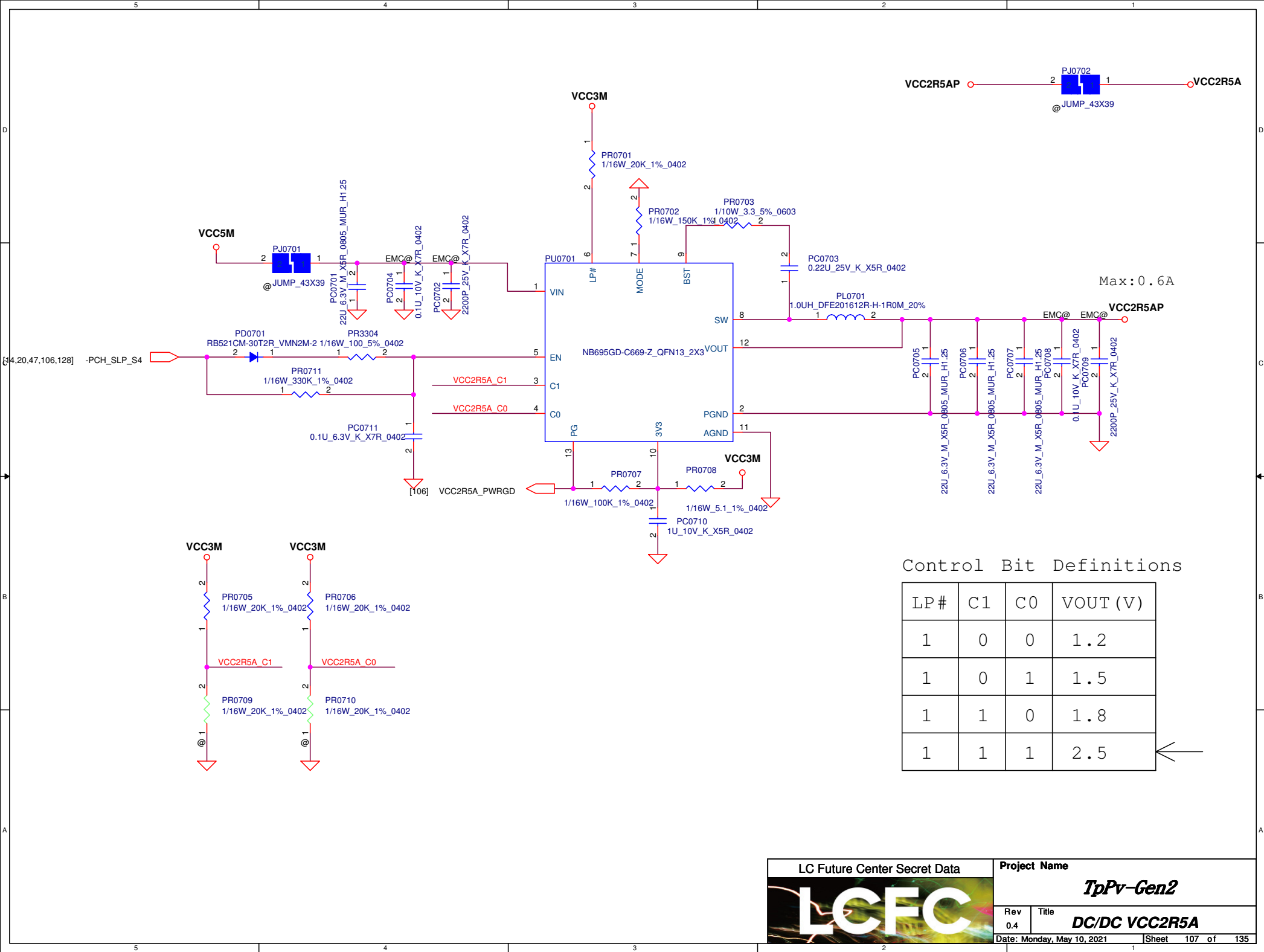




BLANK



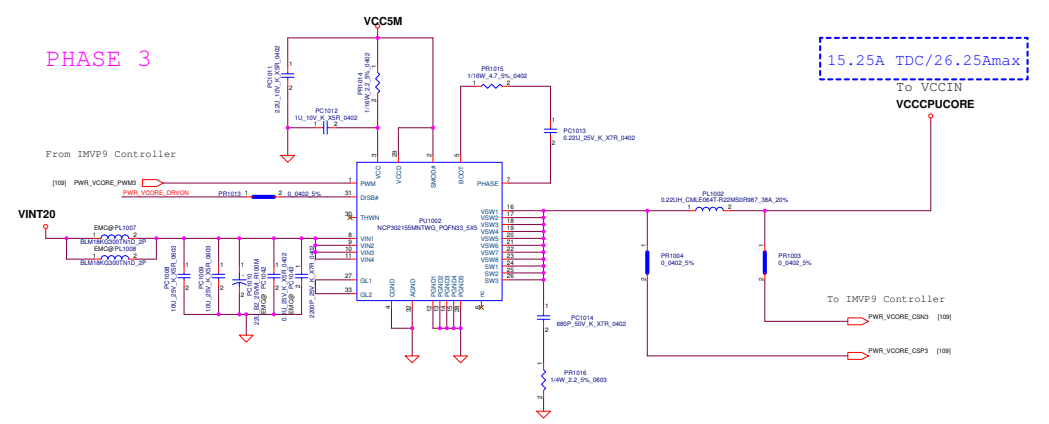
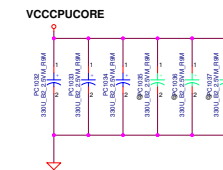




BLANK






[illegible]

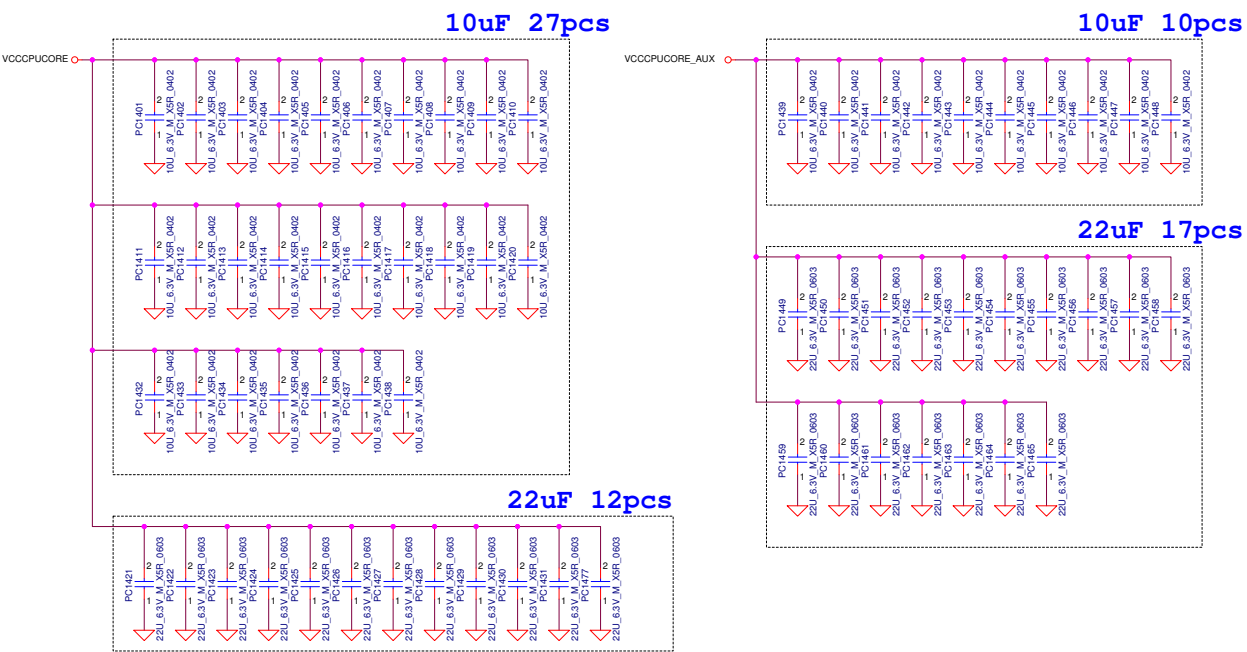
BLANK

BLANK

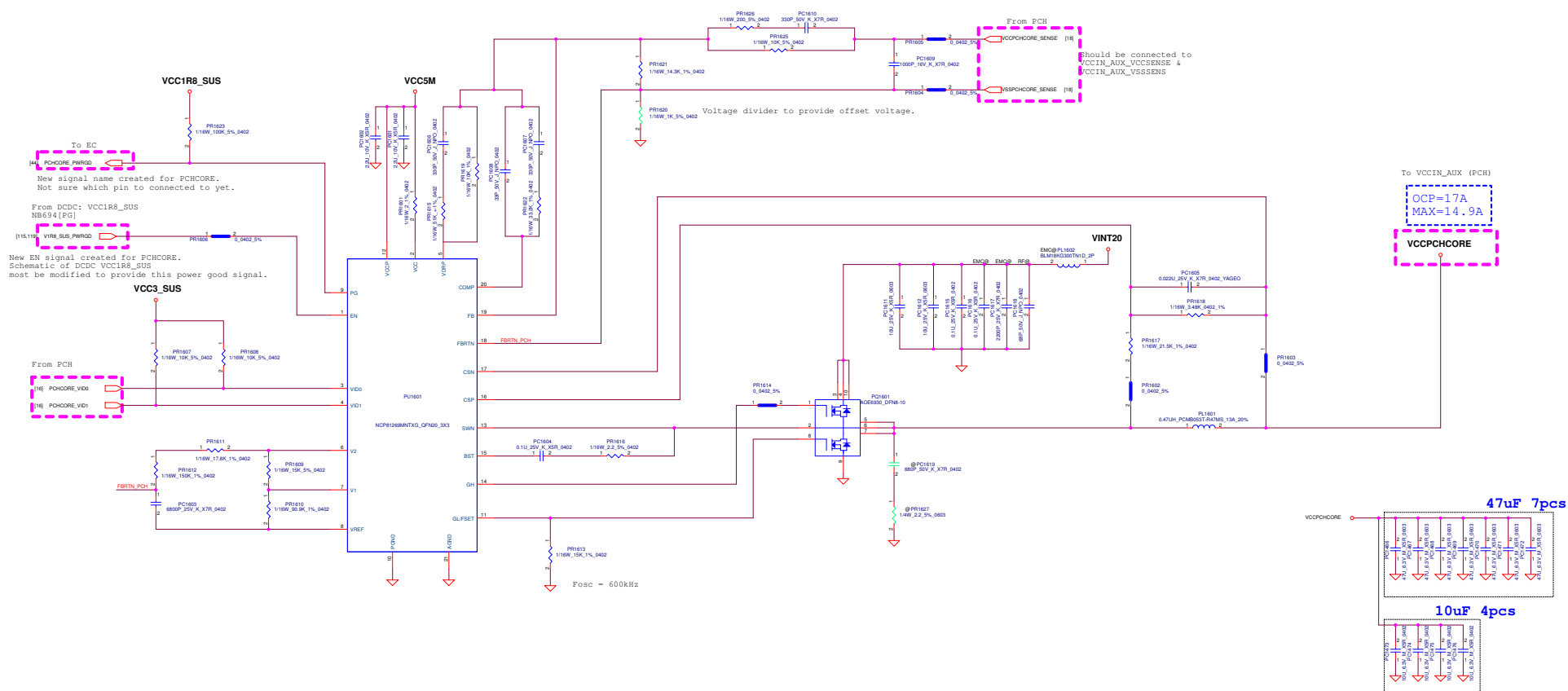
[www.teknisi-indonesia.com](http://www.teknisi-indonesia.com)

LC Future Center Secret Data		Project Name	
		<i><b>IpPv-Gen2</b></i>	
		Rev 0.4	Title <b>BLANK</b>
Date: Monday, May 10, 2021		Sheet	112 of 135

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BLANK

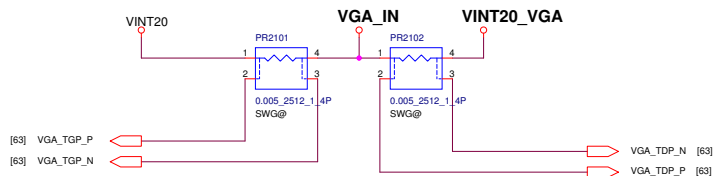
BLANK

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LC Future Center Secret Data		Project Name	
		<i><b>TpPv-Gen2</b></i>	
		Rev 0.4	Title <b>BLANK</b>
Date: Monday, May 10, 2021		Sheet 118 of 135	

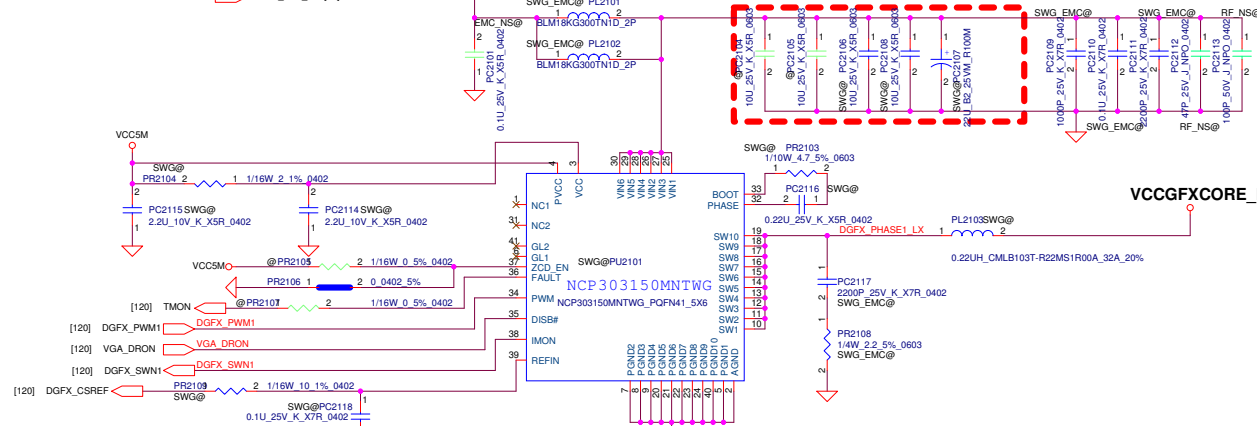






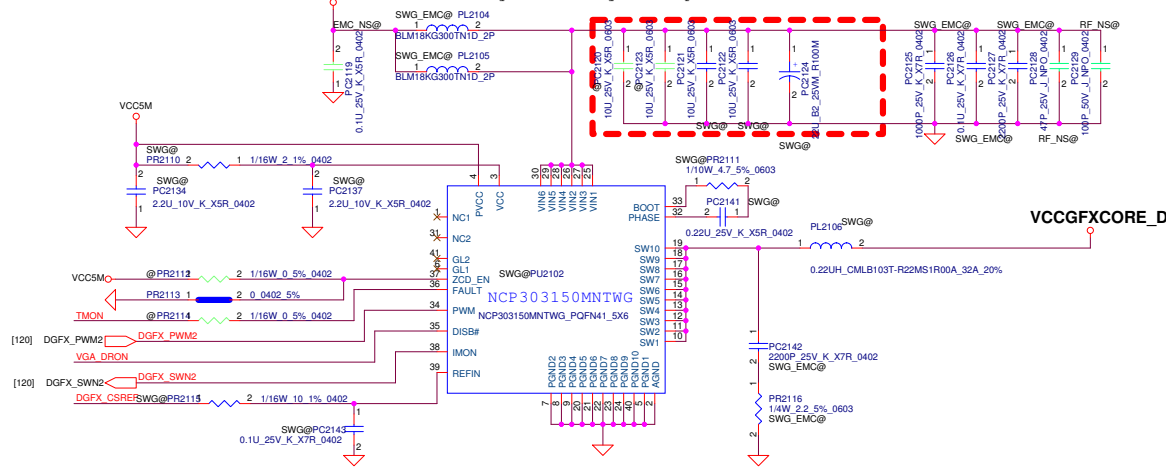
VGA\_IN

MLCCs must be placed symmetrically on Top and Bottom.

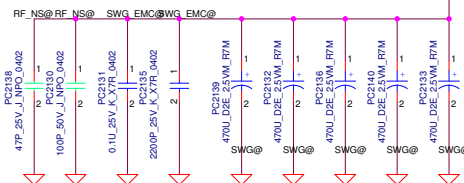


VGA\_IN

MLCCs must be placed symmetrically on Top and Bottom.



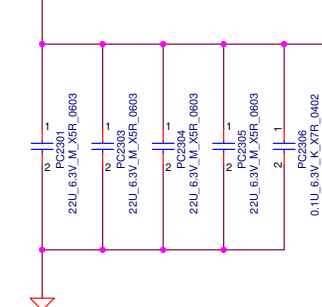
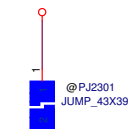
VCCGFXCORE\_D



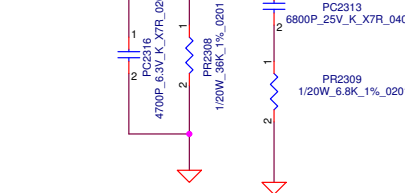
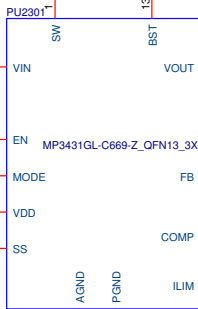
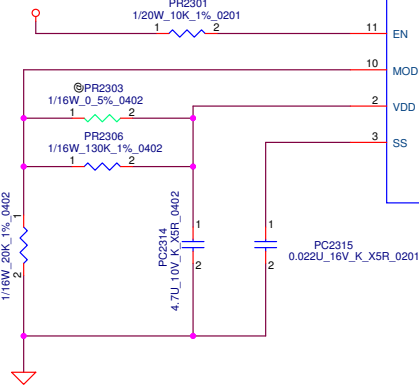
470uF 5pcs



VCC5B

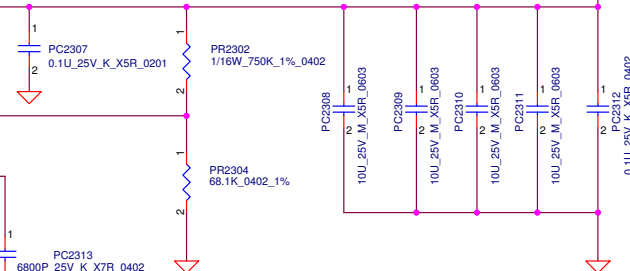


VCC5B



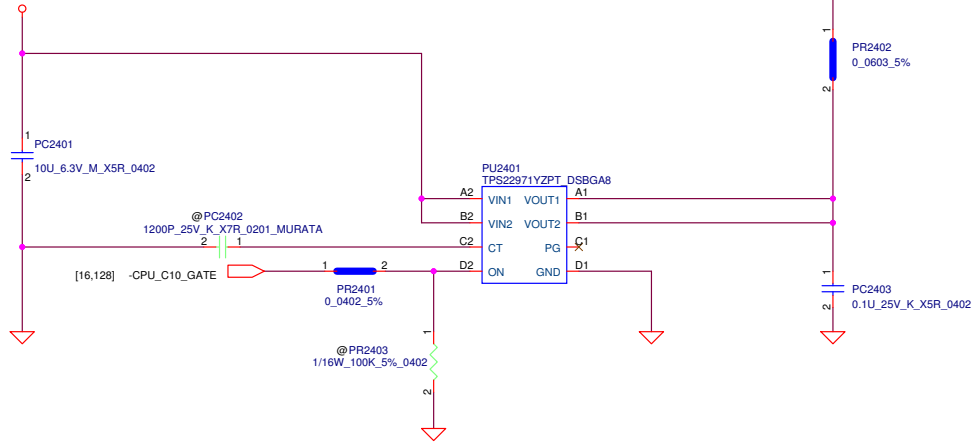
12V/1.2A  
VCC12

VCC12



1.8V

VCC1R8\_SUS

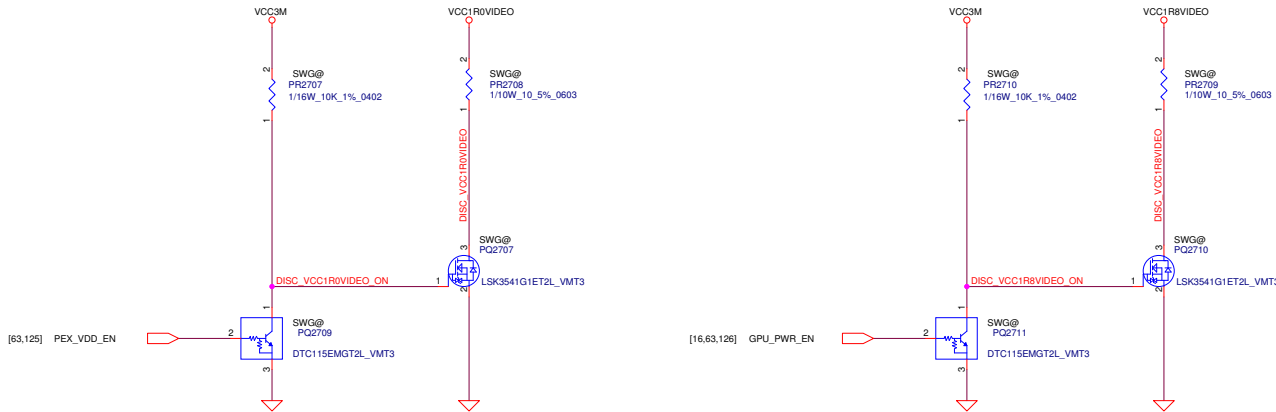
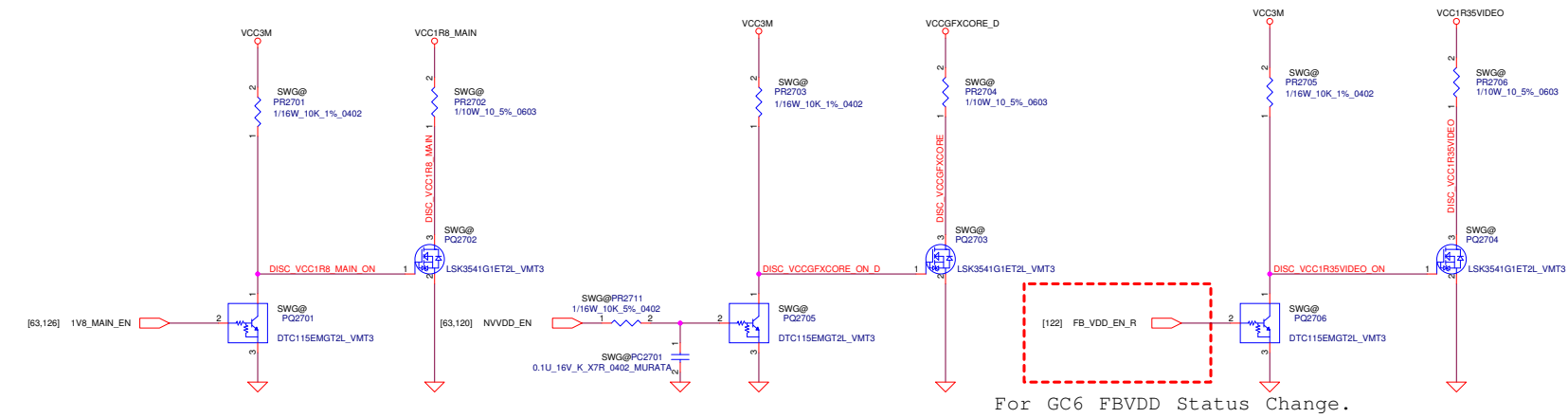


T0 CPU [VCC1P8A]  
VCC1R8A

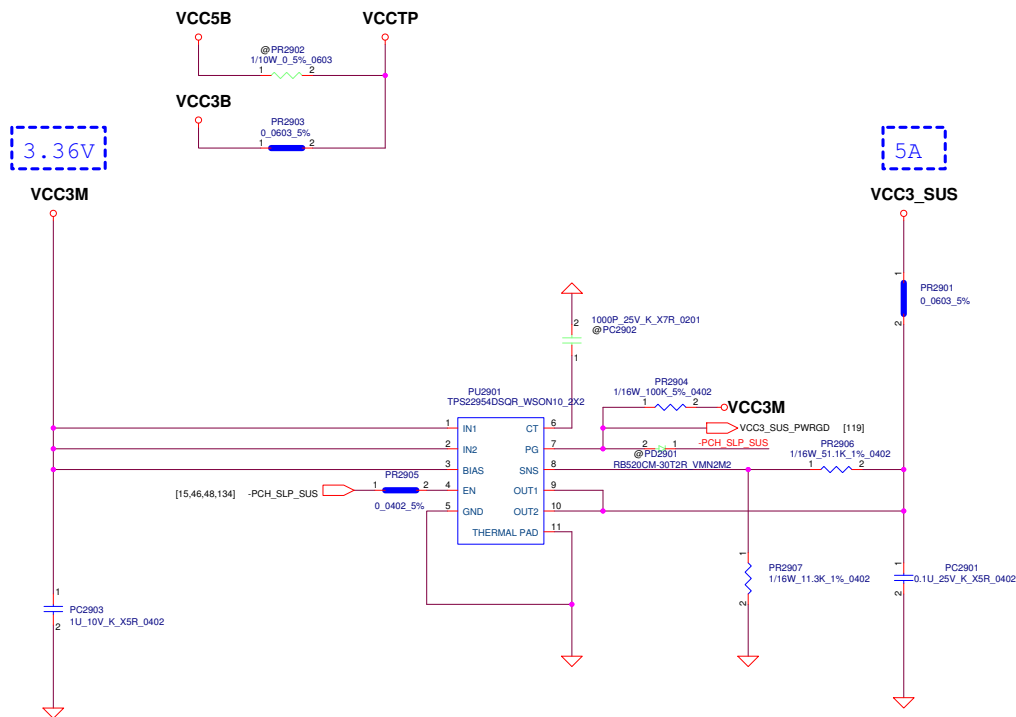


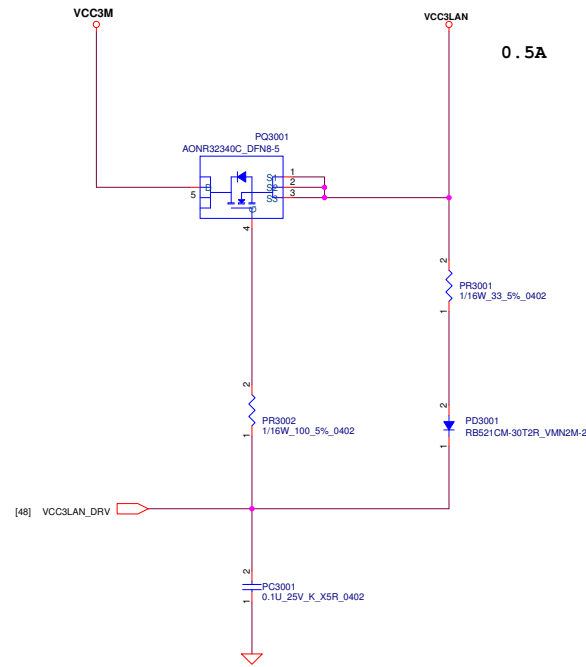


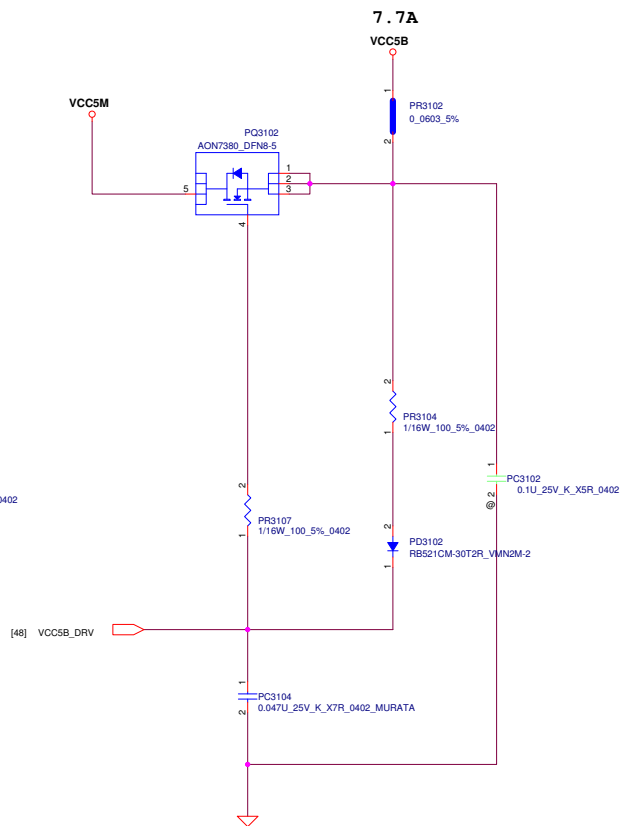
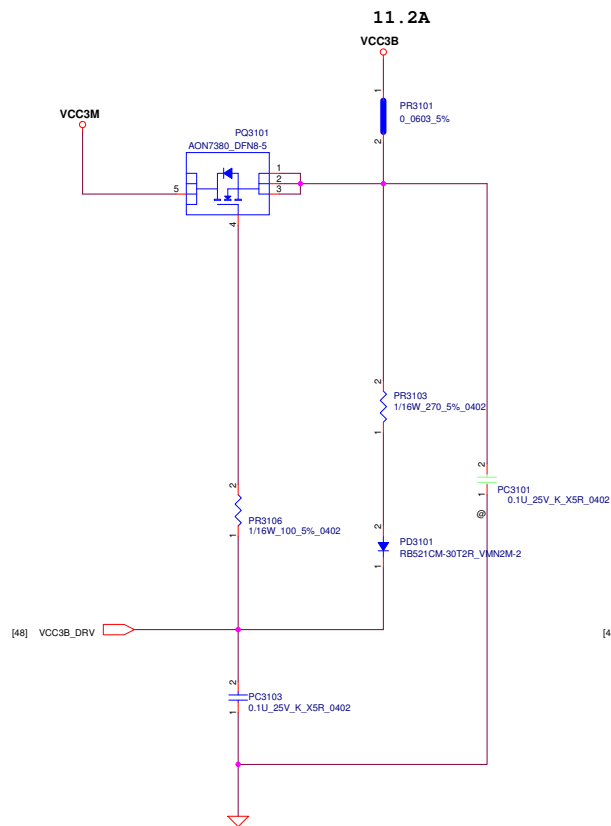


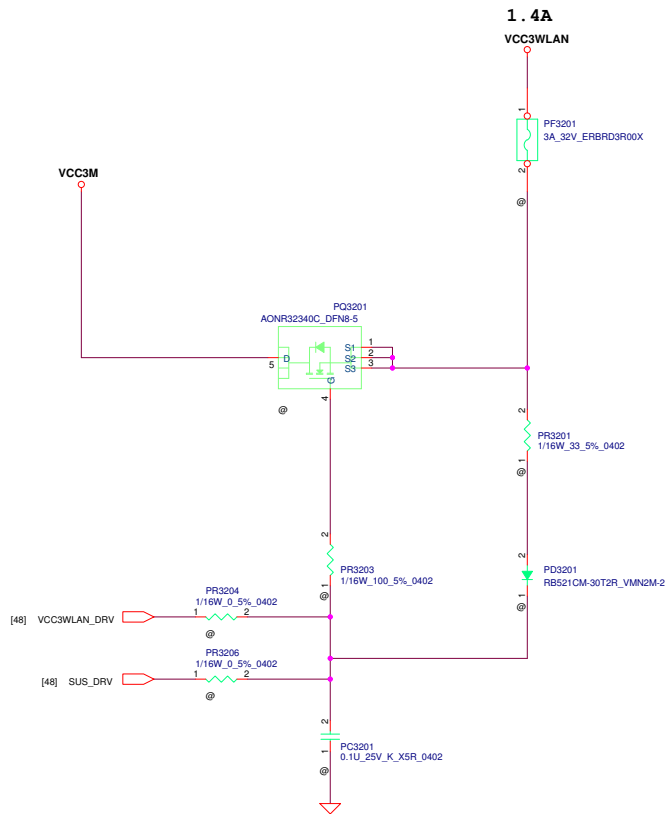






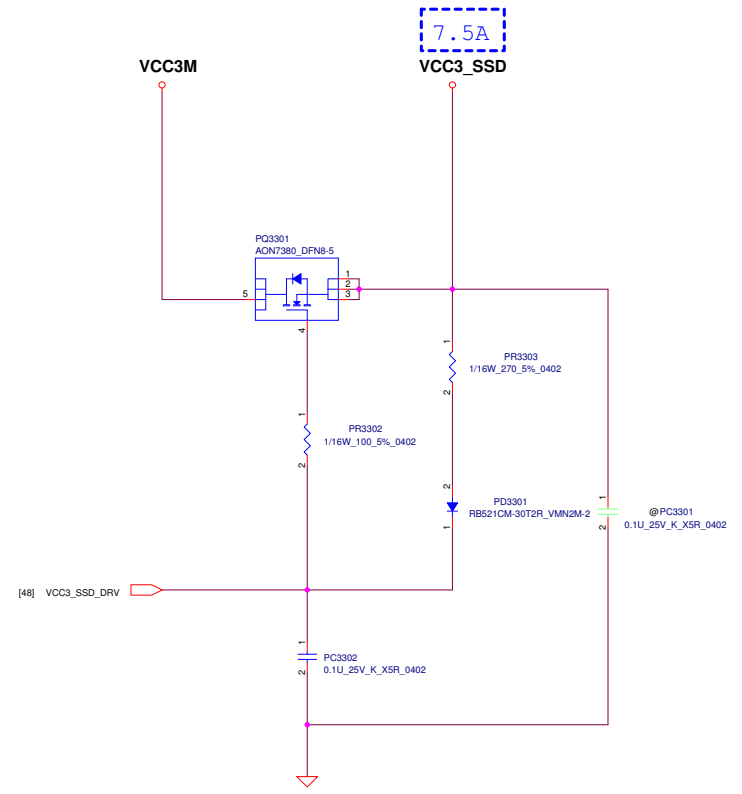


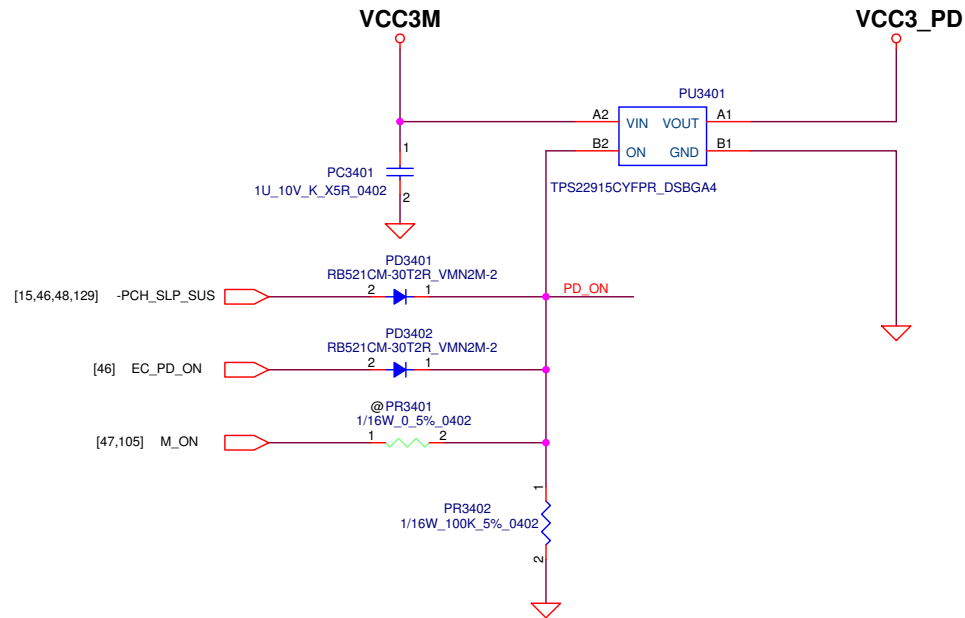







For modern standby





LC Future Center Secret Data		Project Name	
		TpPv-Gen2	
		Rev 0.4	Title LOAD SW VCC3_PD
Date: Monday, May 10, 2021		Sheet 134 of 135	

PR2019  
PQ3@  
1/16W\_2.8K\_1%\_0402

PR2022  
PQ3@  
1/16W\_13.7K\_1%\_0402

PR2021  
PQ3@  
1/16W\_274\_1%\_0402